

# Compal Confidential

## VAL40 MB Schematic Document

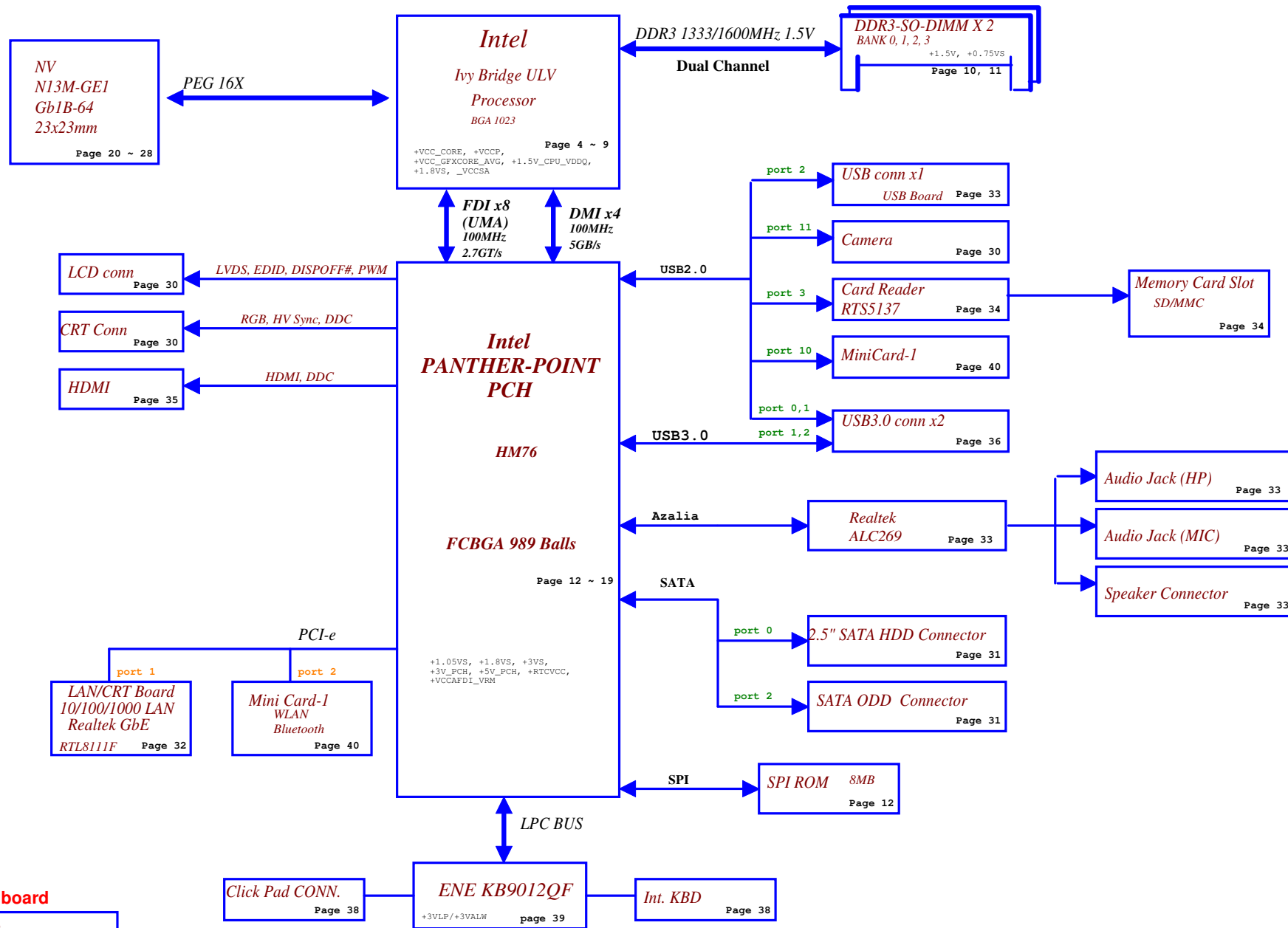
### LA-8226P

Rev: 1.0

2012.07.06

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## VAL40



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				Block Diagram	
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BTO Option Table

BOM Structure	BTO Item
DIS@	VGA componet
GE8@	N13M-GE1_GB1b-64
X76L07@	VRAM Hynix 2Gbx8 256Mx8
GCLK@	G-CLK
GCLKDIS@	G-CLK + SLG3NB300
GCLKUMA@	G-CLK + SLG3NB244
NONGCLK@	NONE G-CLK
AI@	AI Charger
NAI@	Non AI Charger
46@	HDMI royalty rule
I33110@	CPU BGA I3-3110M 2.4G/3M
I32370@	CPU BGA I3-2370M 2.4G/3M
I32350@	CPU BGA I3-2350M 2.3G/3M

CPU BOM Config

I33310@	I3-3110M	CR	2.4G	SA00005M830 (INT I3-3110M 2.4G/3M SR0N2 BGA)
I32370@	I3-2370M	HR	2.4G	SA000059160 (INT I3-2370M 2.4G/3M SR0DQ BGA)
I32350@	I3-2350M	HR	2.3G	SA00004QXA0 (INT I3-2350M 2.3G/3M SR0DQ BGA)

BOM Config : DIS

K45B (i3-3110M) DIS@/GE8@/X7607@/GCLK@/GCLKDIS@/I33110@/NAI@

\* K45B (i3-2370M) DIS@/GE8@/X7607@/GCLK@/GCLKDIS@/I32370@/NAI@

BOM Config : UMA

K45B (i3-3110M) GCLK@/GCLKUMA@/I33110@/NAI@

K45B (i3-2370M) GCLK@/GCLKUMA@/I32370@/NAI@

\* K45B (i3-2350M) GCLK@/GCLKUMA@/I32350@/NAI@

VRAMX8X8



CPU



CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	LPC Debug Port
PCI4	None

Voltage Rails

Power Plane	Description	S0	S3	Deep S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+3VLP	3.3V power rail for 510N power management	ON	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+LAN_IO	3.3V power rail for ethernet	ON	ON	OFF	OFF
+3VS_WLAN	3.3V power rail for WLAN/BT Combo	ON	OFF	OFF	OFF
+3V_PCH	3.3V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+3VS	3.3V power rail for DDR SPI,PCH,HDD,Audio,Card Reader	ON	OFF	OFF	OFF
+3VSG	3.3V power rail for VGA	ON	OFF	OFF	OFF
+LCDVDD	3.3V power rail for LCD	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+5V_PCH	5V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+5VS	5V power rail for HDD,AUDIO,FAN,Touch PAD	ON	OFF	OFF	OFF
+5VS_ODD	5V power rail for SATA ODD	ON	OFF	OFF	OFF
+1.8VS	1.8V power rail for CPU,PCH	ON	OFF	OFF	OFF
+1.05VS	1.05V power rail for PCH	ON	OFF	OFF	OFF
+VCCP	1.05V power rail for CPU VCCIO,PCH	ON	OFF	OFF	OFF
+1.05VSG	1.05V power rail for N13P	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR3 system memory	ON	ON	ON	OFF
+1.5V_CPU_VDDQ	1.5V power rail CPU VDDQ	ON	OFF	OFF	OFF
+1.5VSG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+1.5VS	1.5V power rail for PCH,WLAN/BT combo	ON	OFF	OFF	OFF
+0.75VS	0.75V power rail for DDR VREF	ON	OFF	OFF	OFF
+VCCSA	VCCSA for CPU system agent	ON	OFF	OFF	OFF
+VCC_CORE	CORE Voltage for CPU	ON	OFF	OFF	OFF
+VCC_GFXCORR_AXG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+VGA_CORE	CORE Voltage for N13P Graphics	ON	OFF	OFF	OFF

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD WLAN
Lane 3	None
Lane 4	USB3.0 controller
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None



PCH

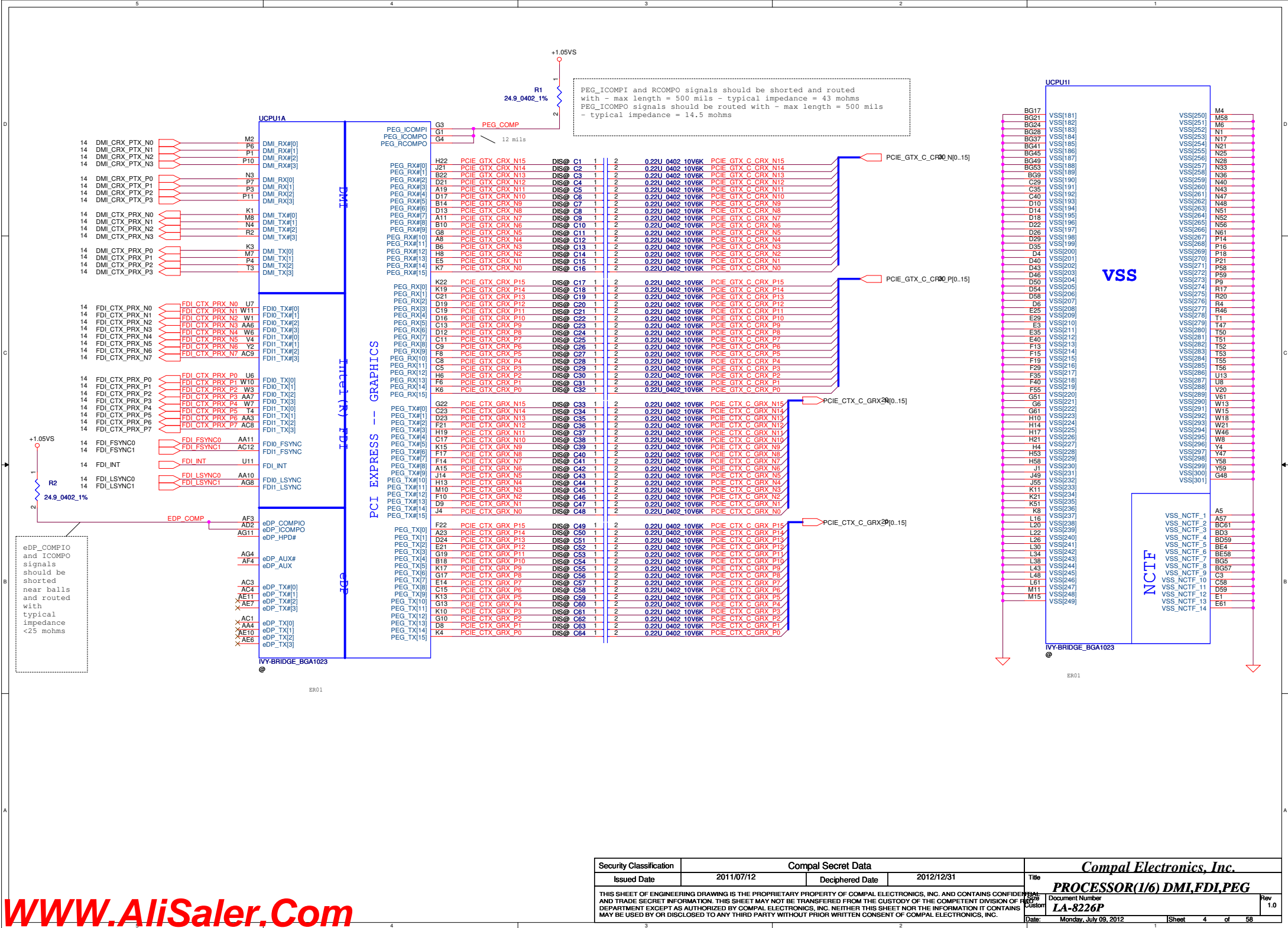
USB2 PORT	DESTINATION
0	USB2.0+3.0
1	USB2.0+3.0
2	USB2
3	Card Reader
4	None
5	None
6	None
7	None
8	None
9	None
10	JMINI1 (WLAN) Bluetooth
11	CAMERA
12	None
13	None

SMBUS Control Table

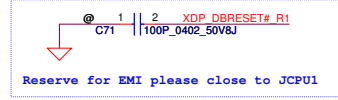
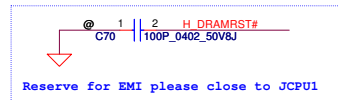
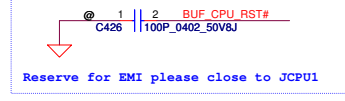
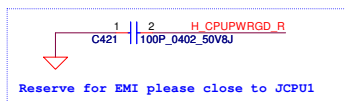
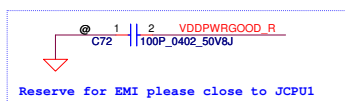
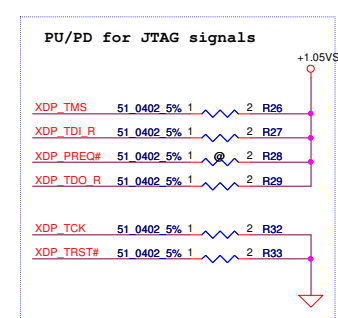
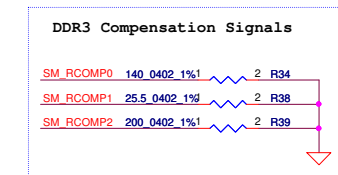
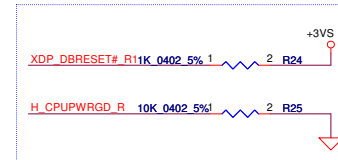
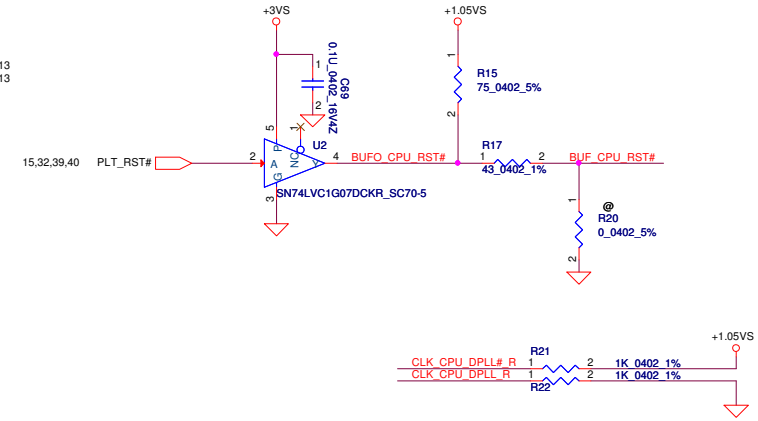
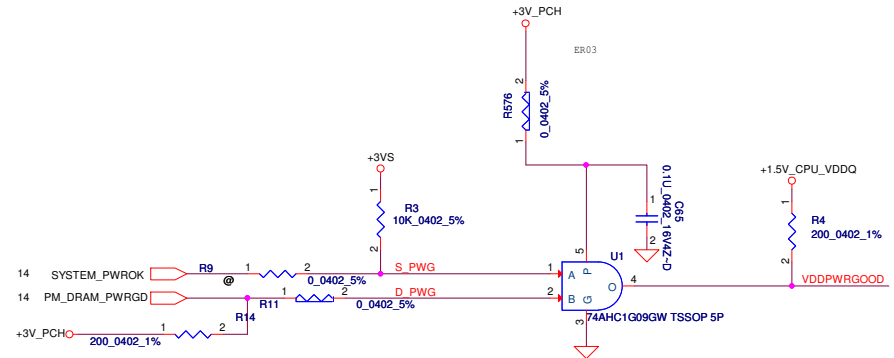
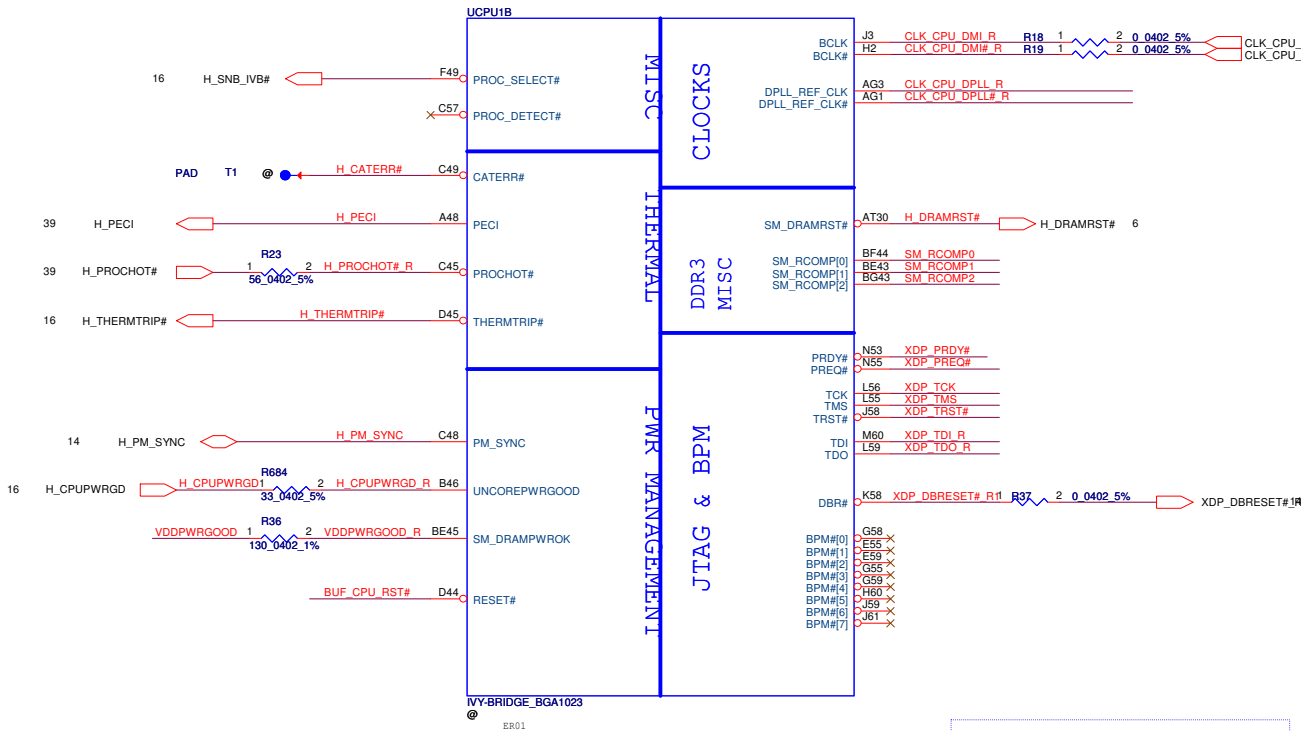
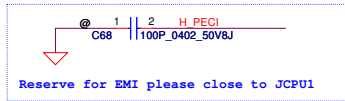
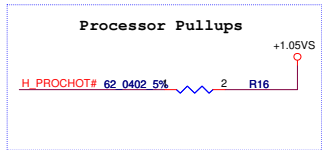
	SOURCE	MINI1	BATT	PCH	EC	SODIMM	DGPU
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V	X	X	V
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	X	X	V	X
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	V	X	V

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	CLK_SD_48M
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	USB3.0 controller	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

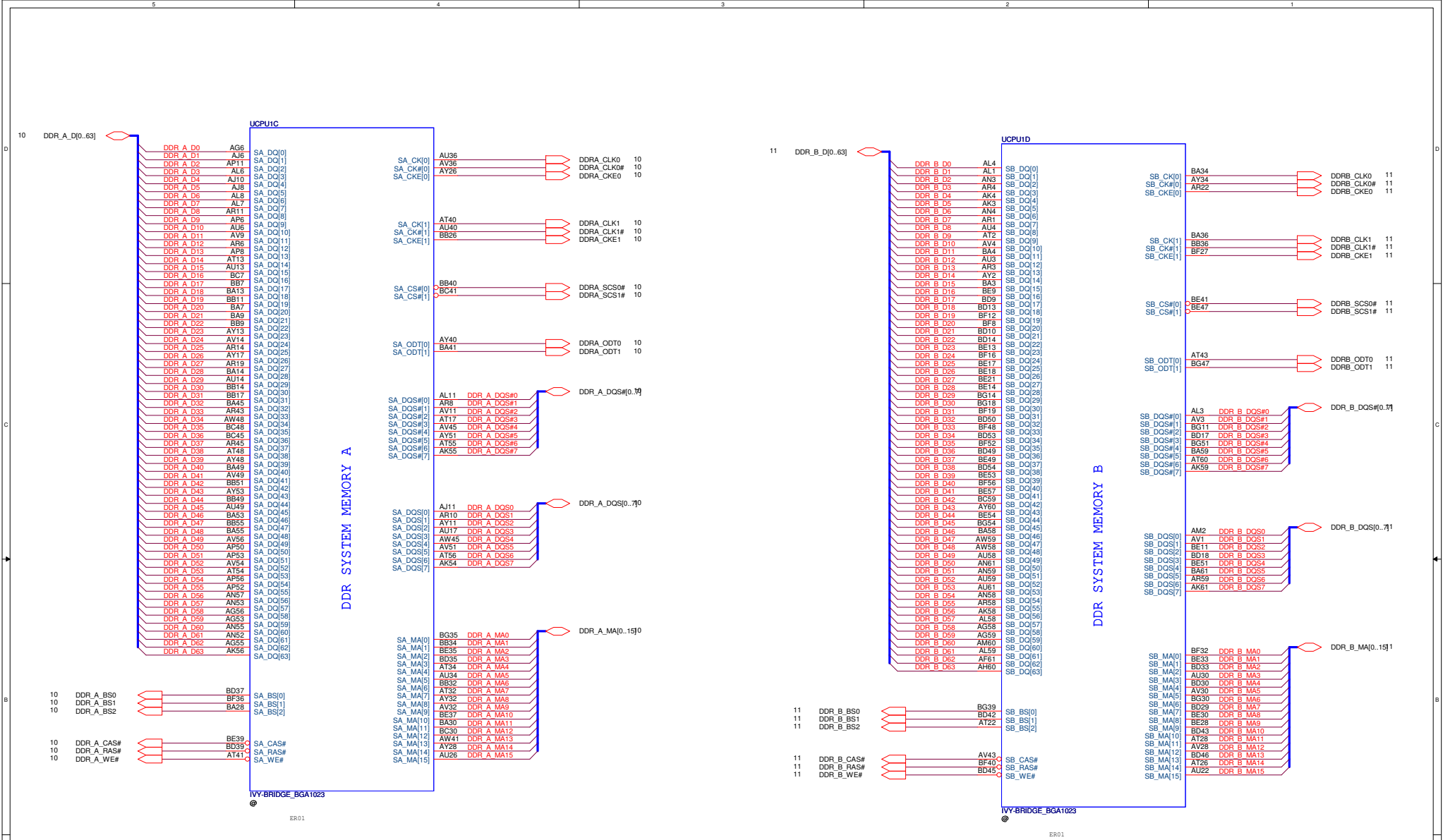
Symbol Note :  
 : means Digital Ground  
 : means Analog Ground



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5 H\_DRAMRST# H\_DRAMRST#

Q6 BSS138\_SOT23

4.99K\_0402\_1% R42

0.0402\_5% R44

EC\_DRAMRST\_CTRL\_PCH

Instant ON

0.047U\_0402\_16V4Z C73

0.0402\_5% R40

1K\_0402\_5% R41

DDR3\_DRAMRST#10,11

+1.5V

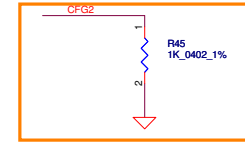
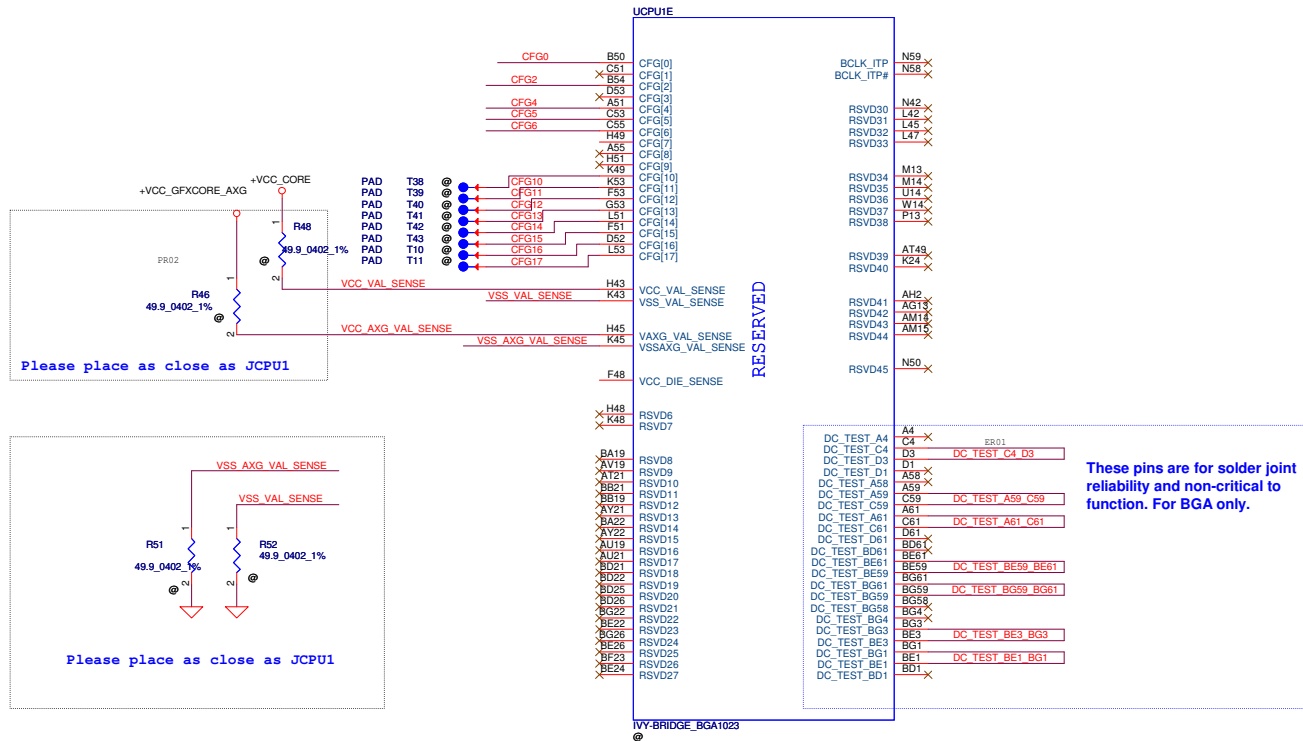
1K\_0402\_5% R40

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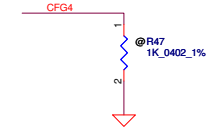
WW.AliSaler.Com

PROCESSOR(3/6) DDRIII

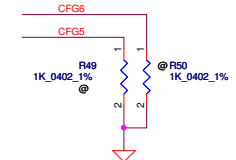
## CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

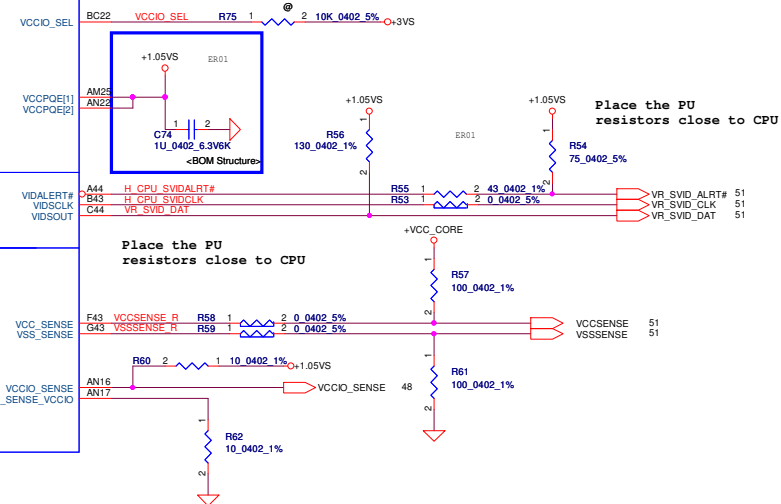


Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

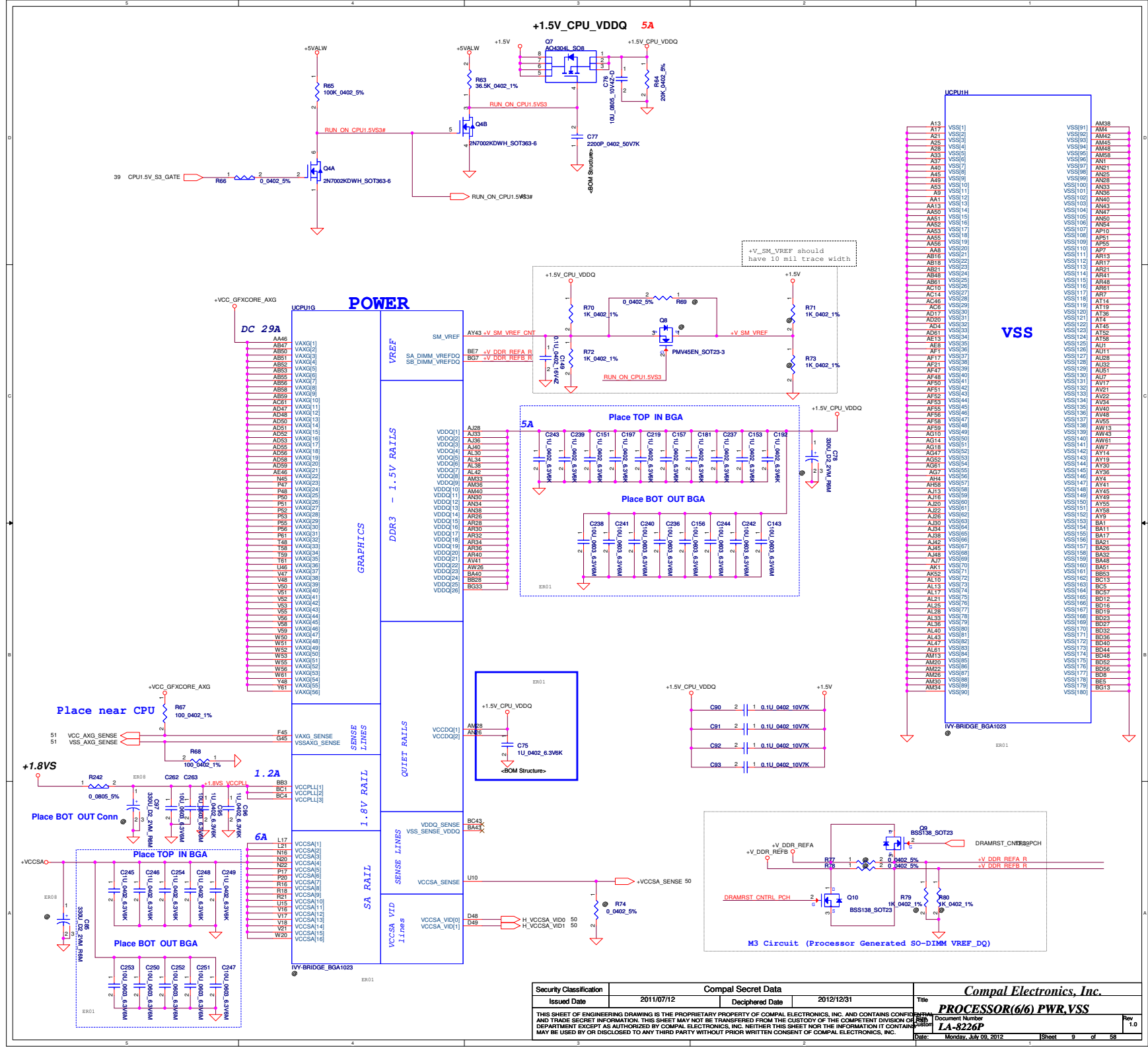


PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled





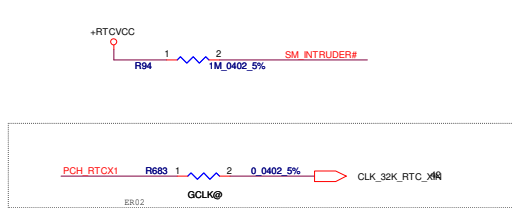
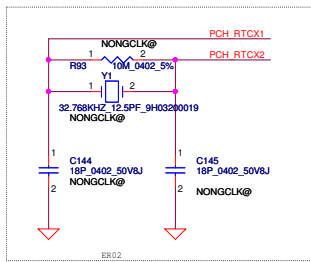




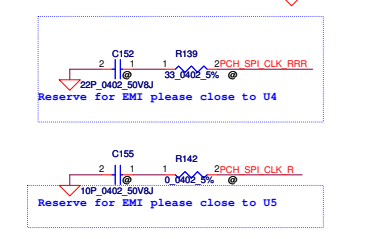
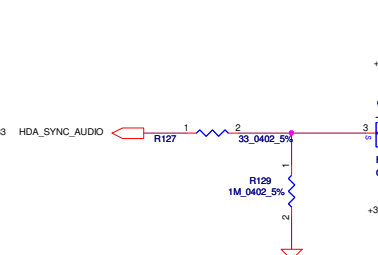
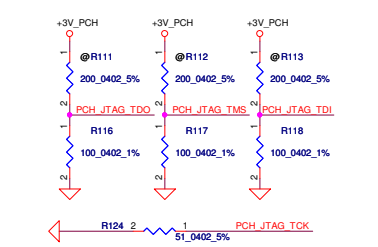
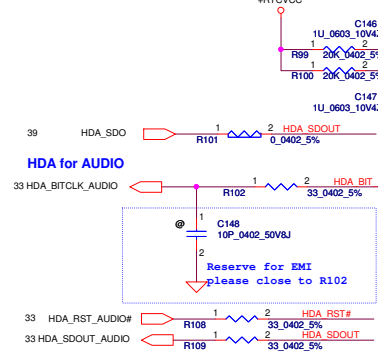
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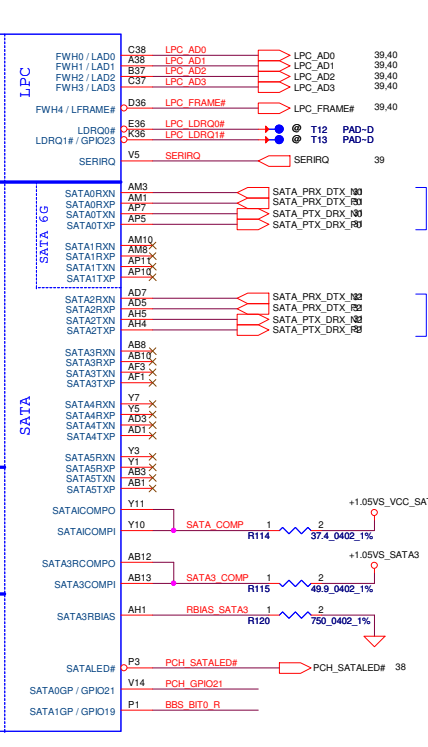
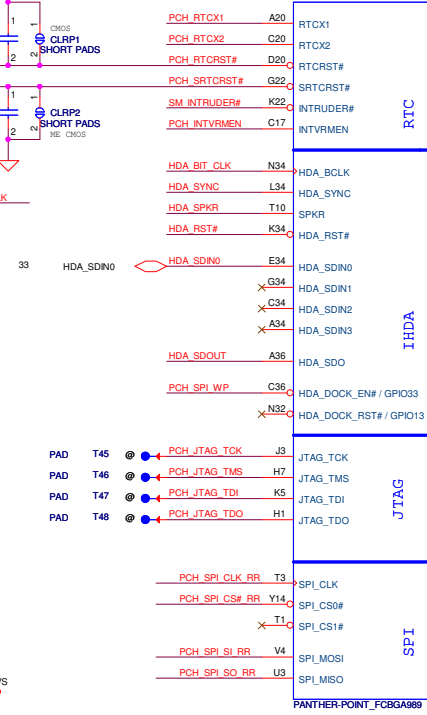




far away hot spot

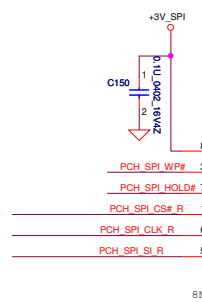


CLRP1 & CLRP2 place near DIMM

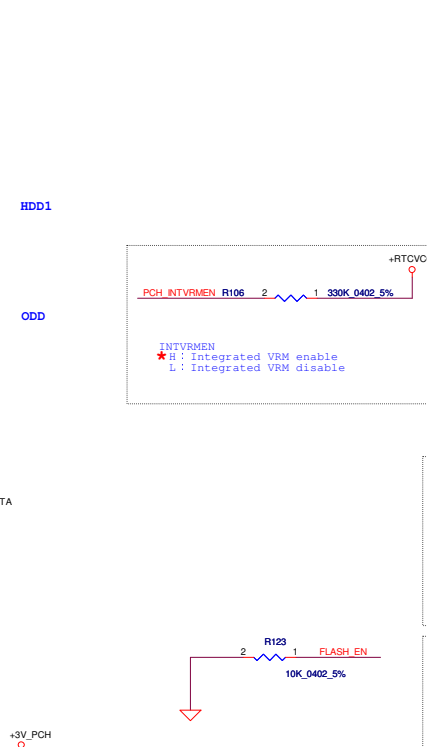


PANTHER-POINT\_FCBGA989

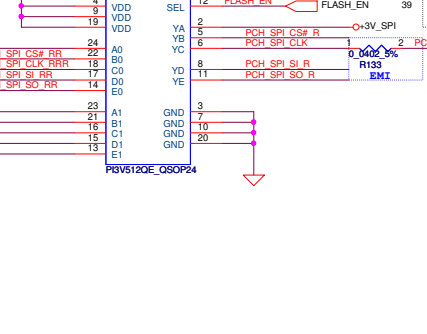
SPI ROM (8MByte)



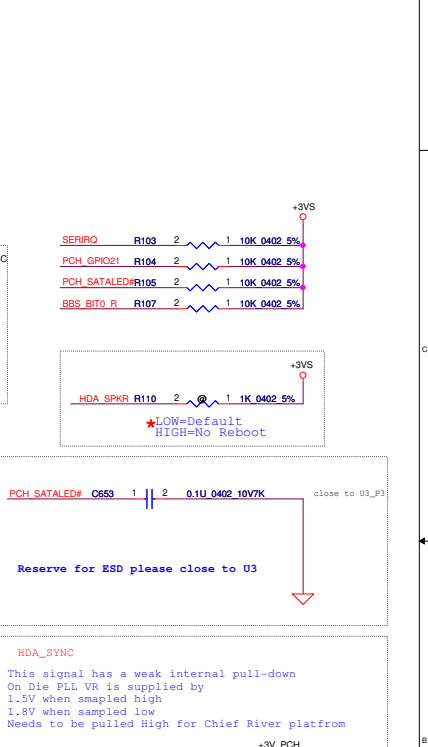
8M ROM-SA000039A20



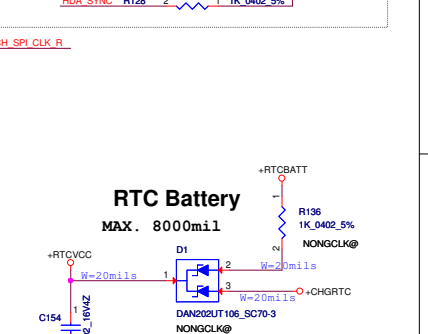
PANTHER-POINT\_FCBGA989



PANTHER-POINT\_FCBGA989



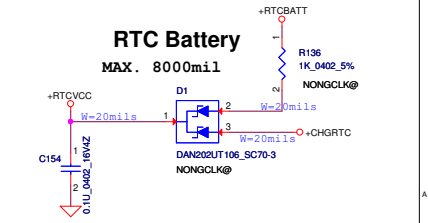
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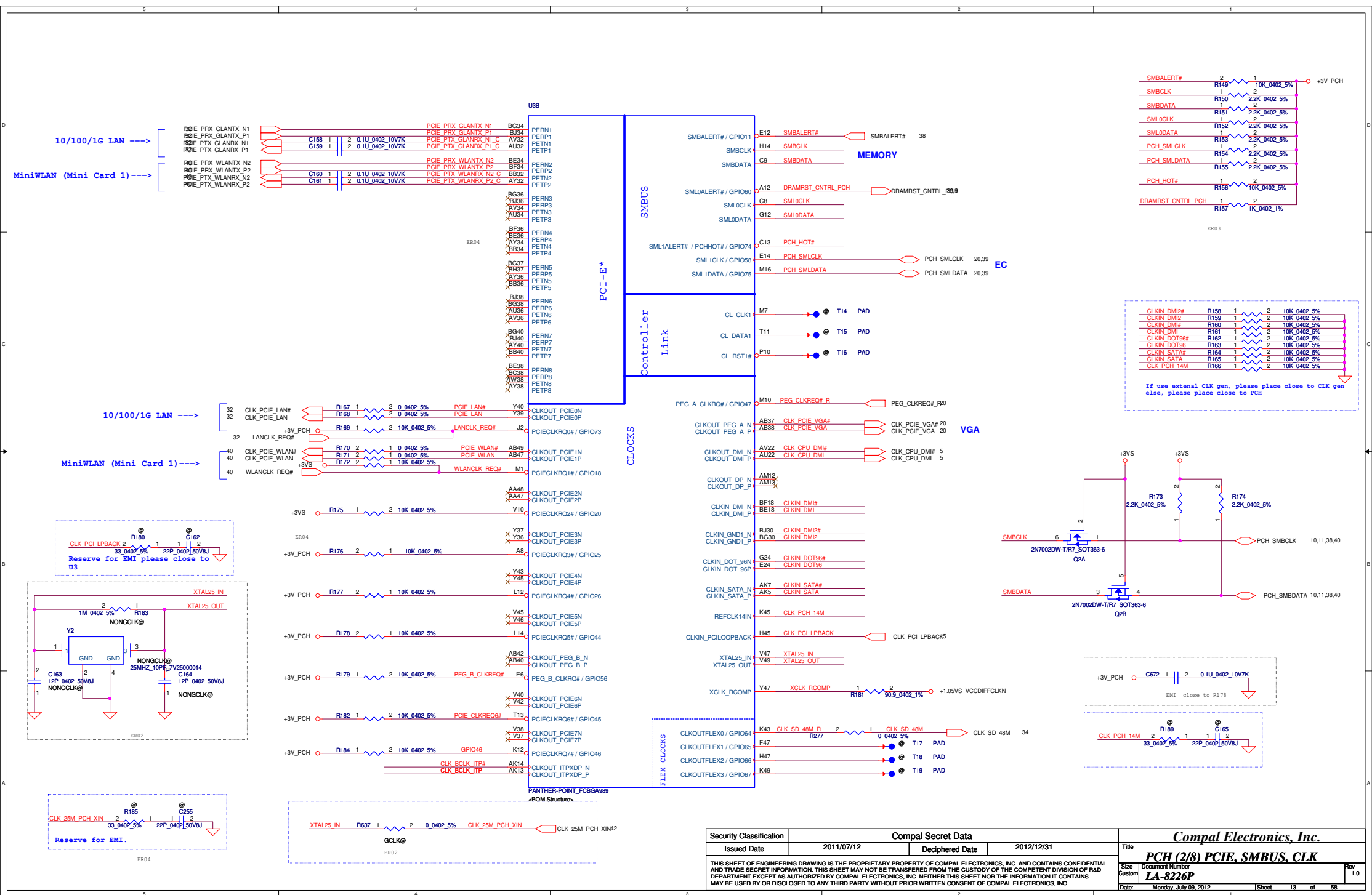
PANTHER-POINT\_FCBGA989

RTC Battery

MAX. 8000mili

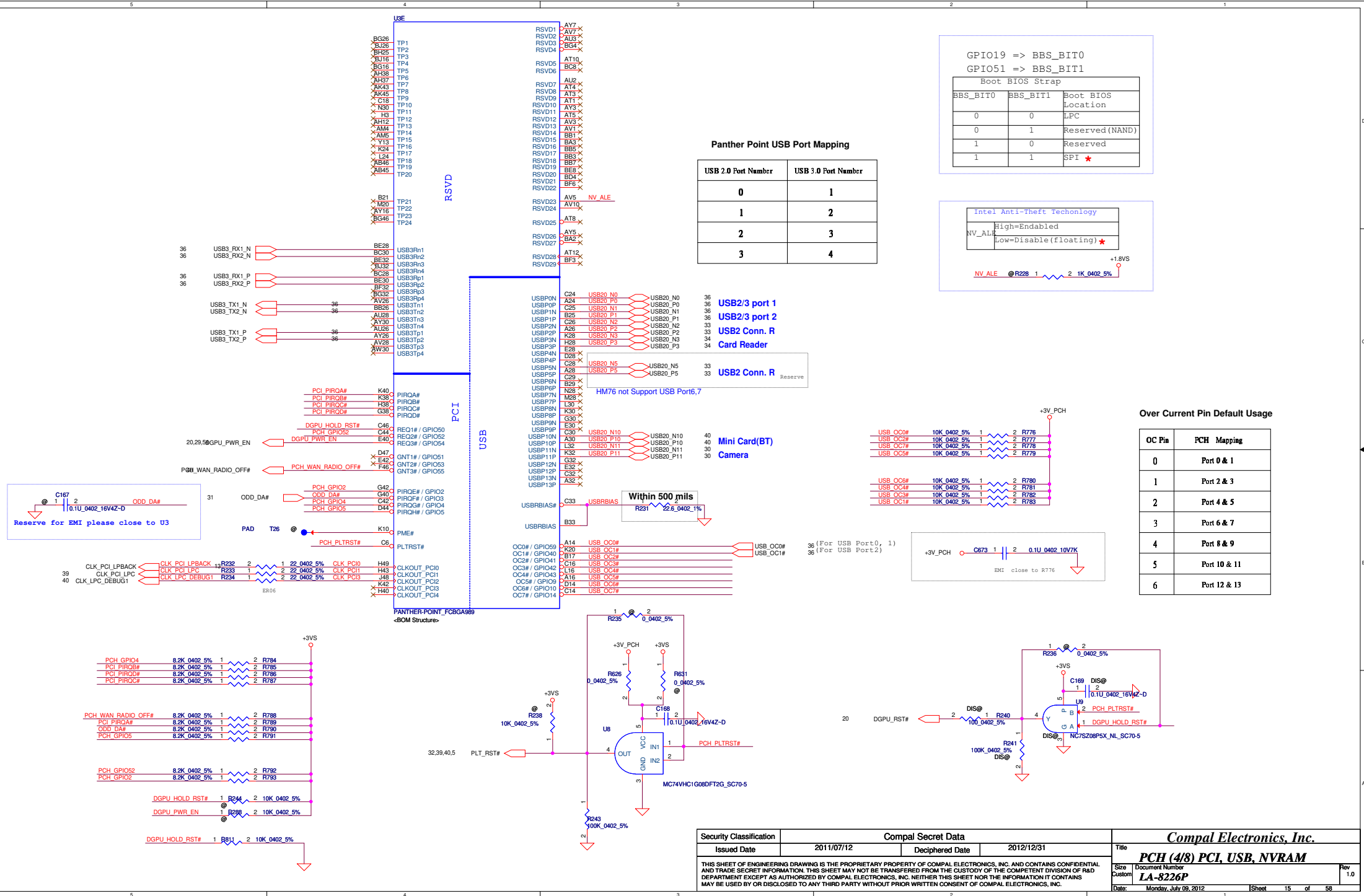


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Panther Point USB Port Mapping

USB 2.0 Port Number	USB 3.0 Port Number
0	1
1	2
2	3
3	4

GPIO19 => BBS\_BIT0  
GPIO51 => BBS\_BIT1

Boot BIOS Strap		
BBS_BIT0	BBS_BIT1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	Reserved
1	1	SPI ★

Intel Anti-Theft Technology

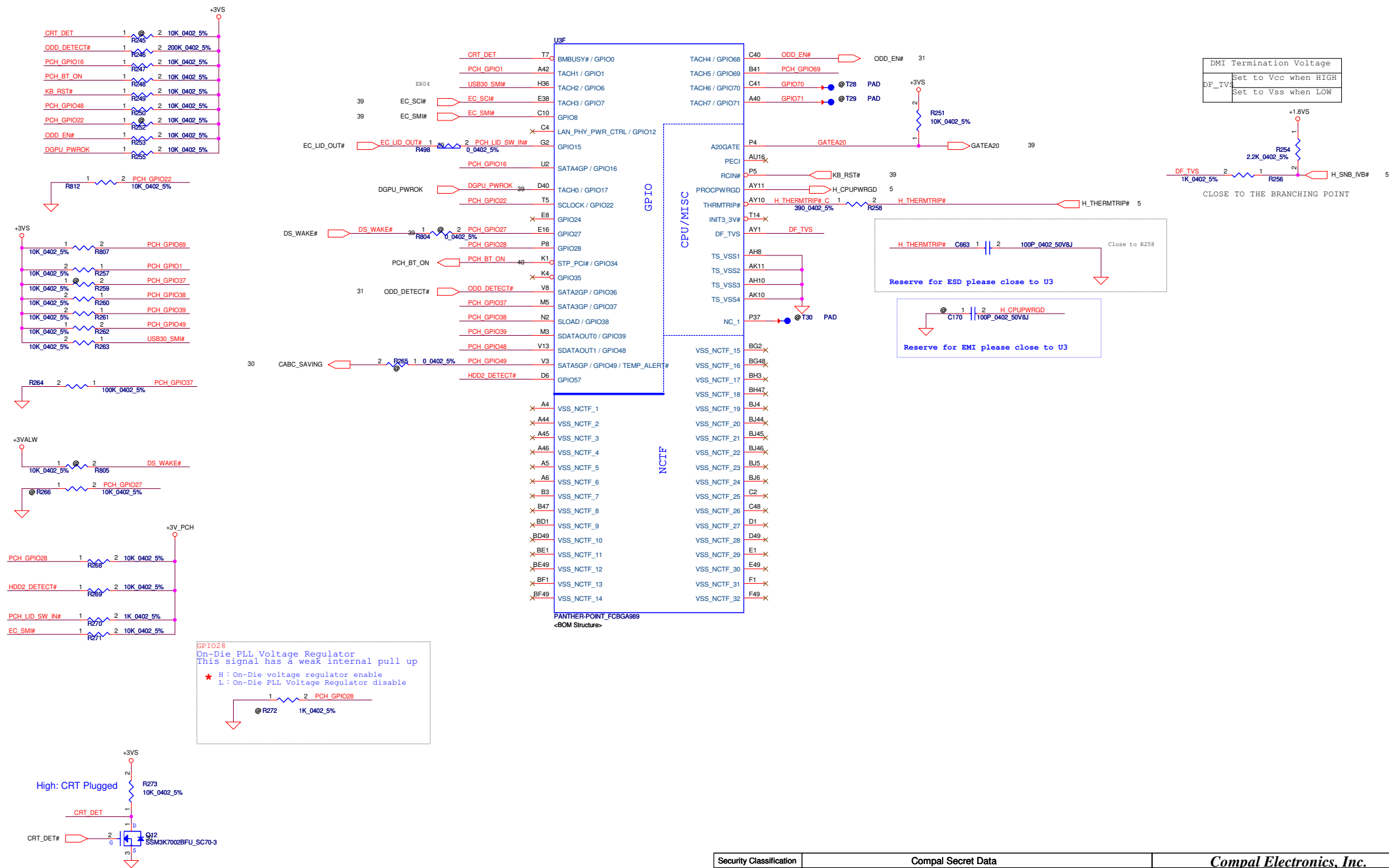
NV_ALE	High=Enabled	Low=Disable(floating) ★
--------	--------------	-------------------------

NV\_ALE @ R228 1 2 1K 0402 5% +1.8VS

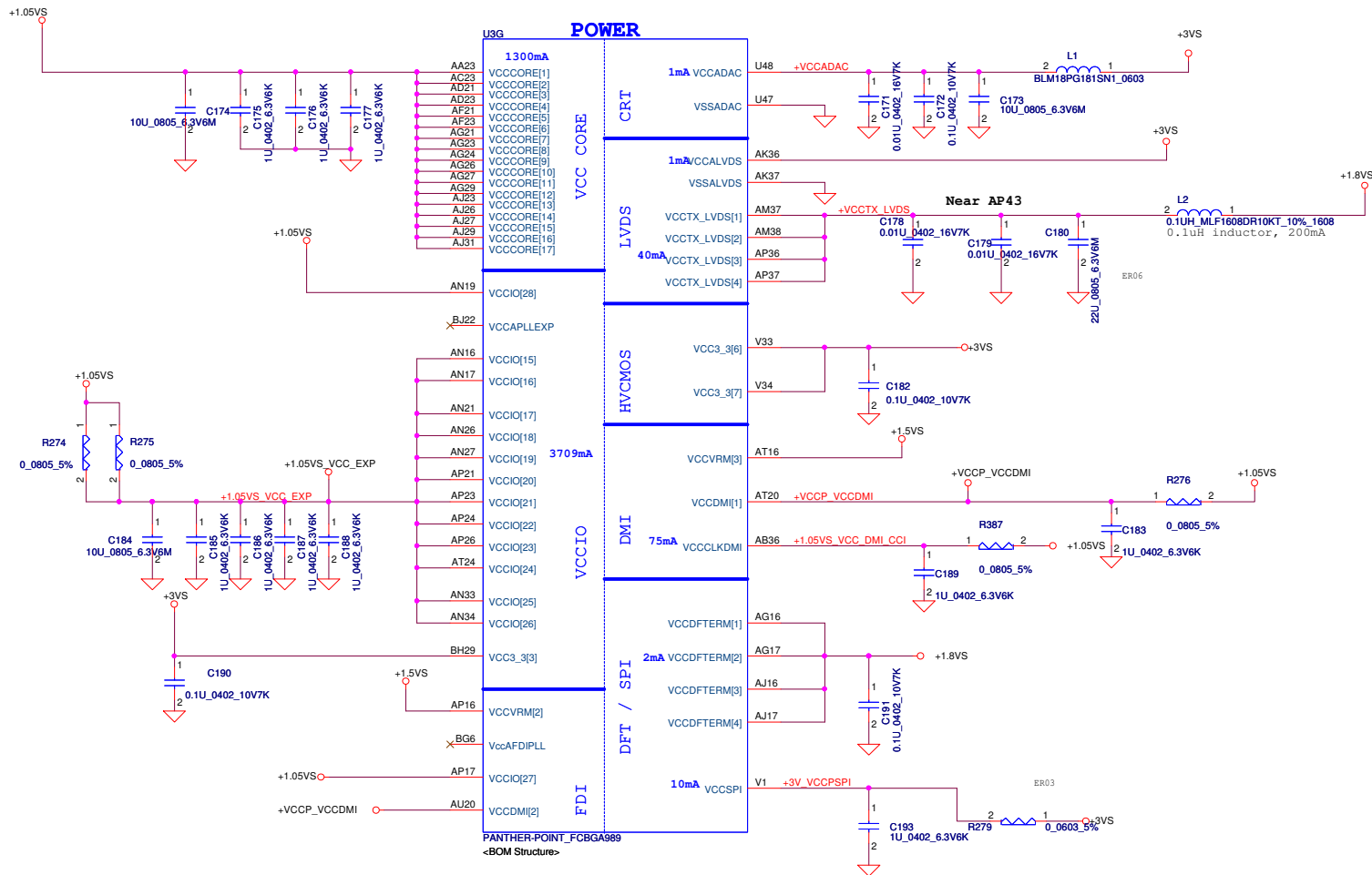
Over Current Pin Default Usage

OC Pin	PCH Mapping
0	Port 0 & 1
1	Port 2 & 3
2	Port 4 & 5
3	Port 6 & 7
4	Port 8 & 9
5	Port 10 & 11
6	Port 12 & 13



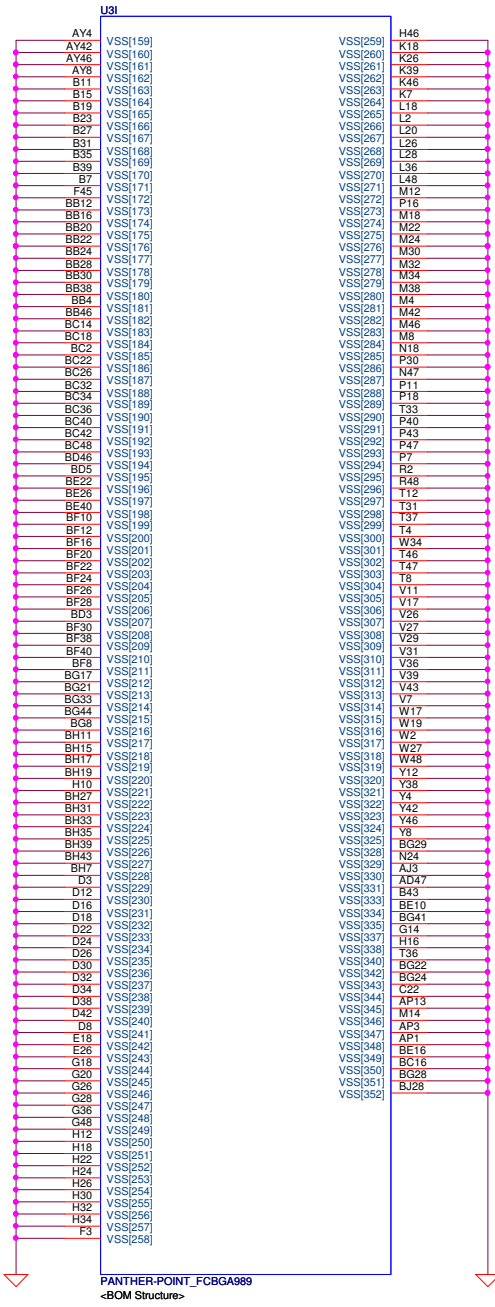
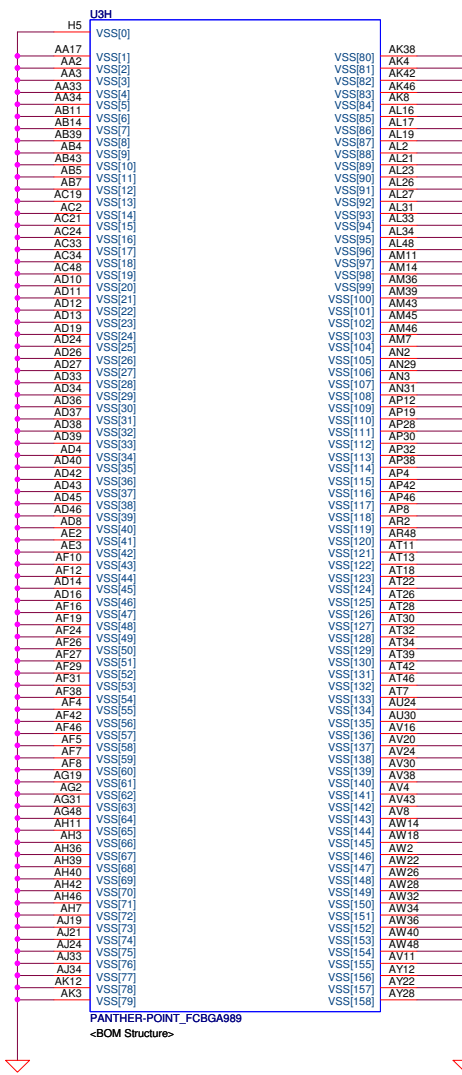


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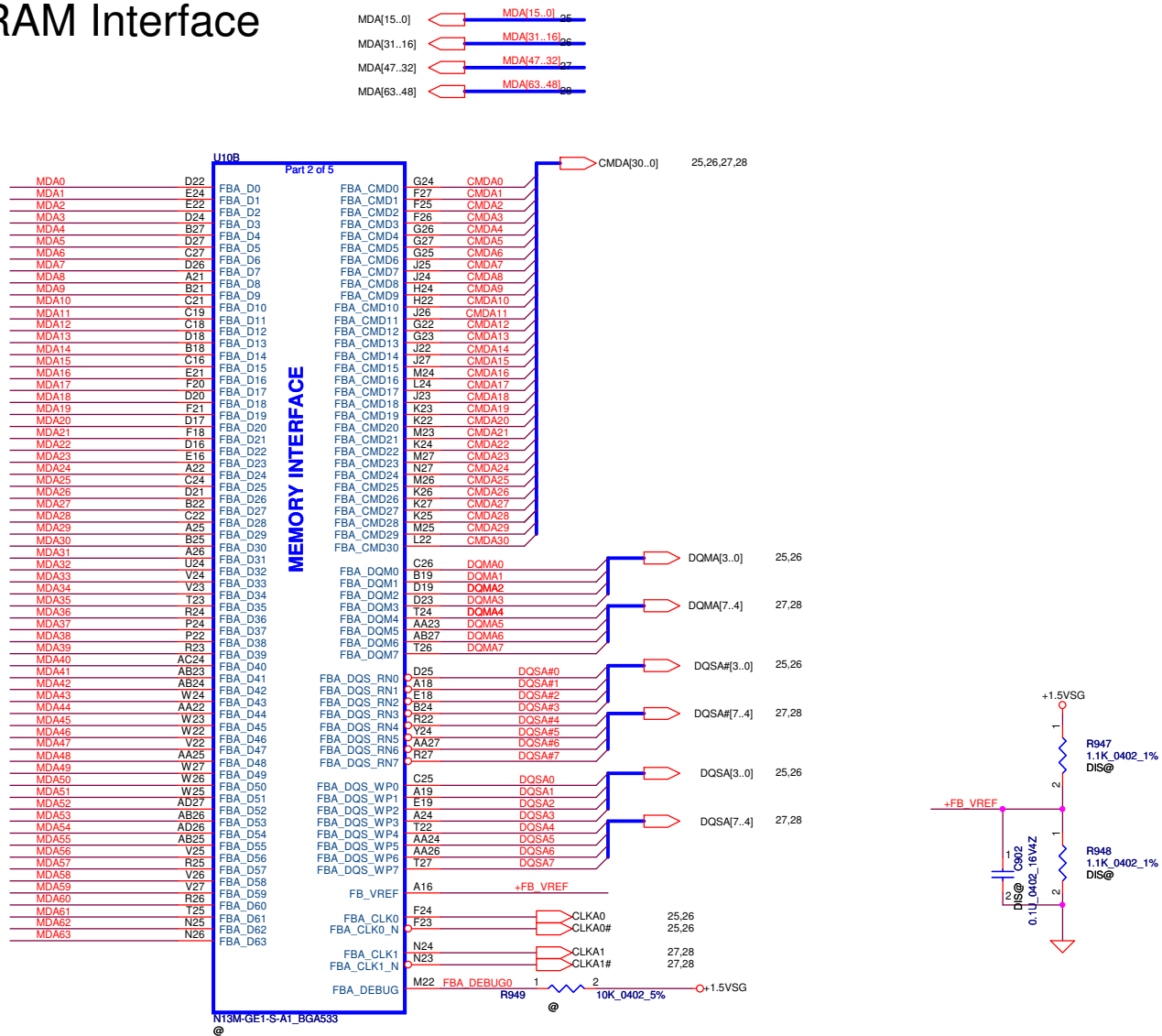
PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



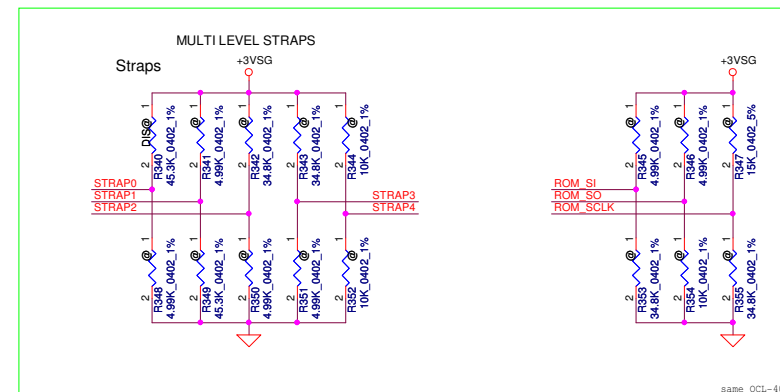




## VRAM Interface



Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>N13M VRAM 2/9</b>	
Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	
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				Custom	<b>LA-8226P</b> Date: Monday, July 09, 2012
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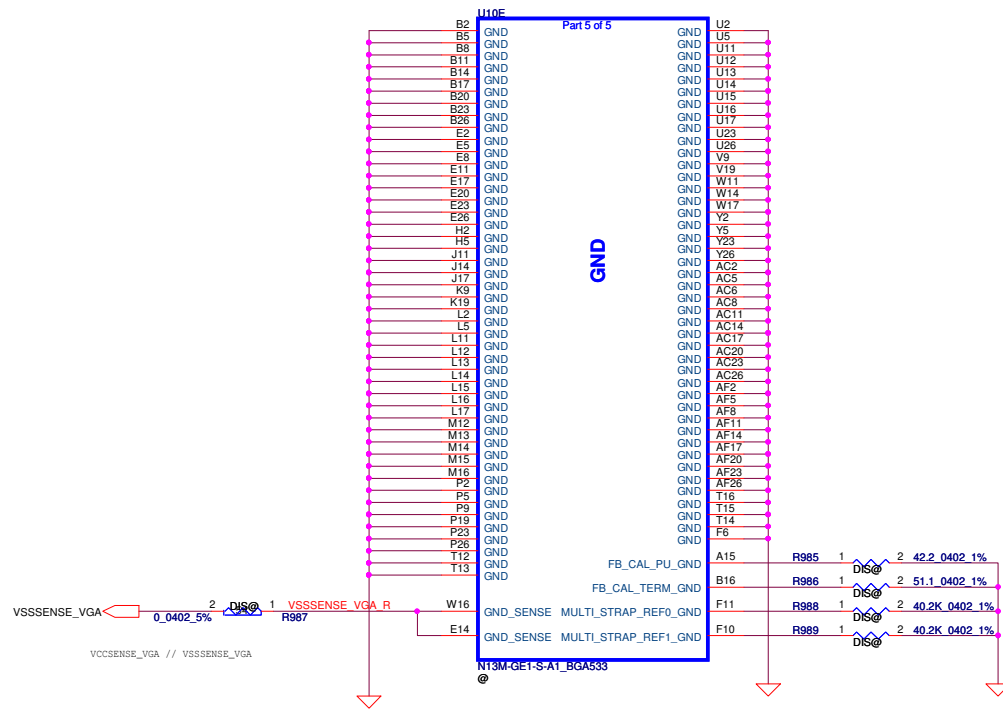
For N13M-GE1 GB1b-64\_256Mx8 strap table

	GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
Cancel	N13M-GE1	800 MHz	256M* 8" 8 2GB	ELPIDA SA000056P00 EDJ2108BCSE-DJ-F	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 5K	R PU 10K	R PU 5K
	N13M-GE1	800 MHz	256M* 8" 8 2GB	HYNIX SA000056H00 H5TQ2G38C3FR-9C0	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 10K	R PU 10K	R PU 5K

```
256M*8*8
1.SA000056000
DDR3 1600 256*8 1.5V FBGA78
HYNIX/H5TQ2G83CFR-PBC
2.SA000056P00
DDR3 1600 256*8 1.5V FBGA78
ELPIDA/EDJ2108BDBG-GN-F
```



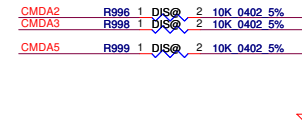
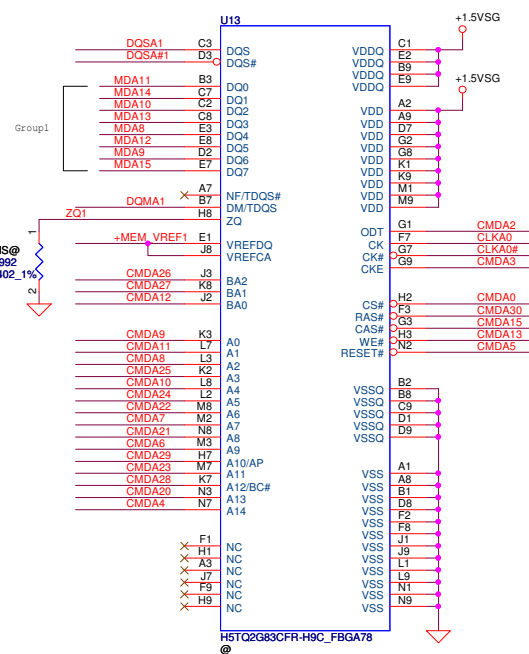
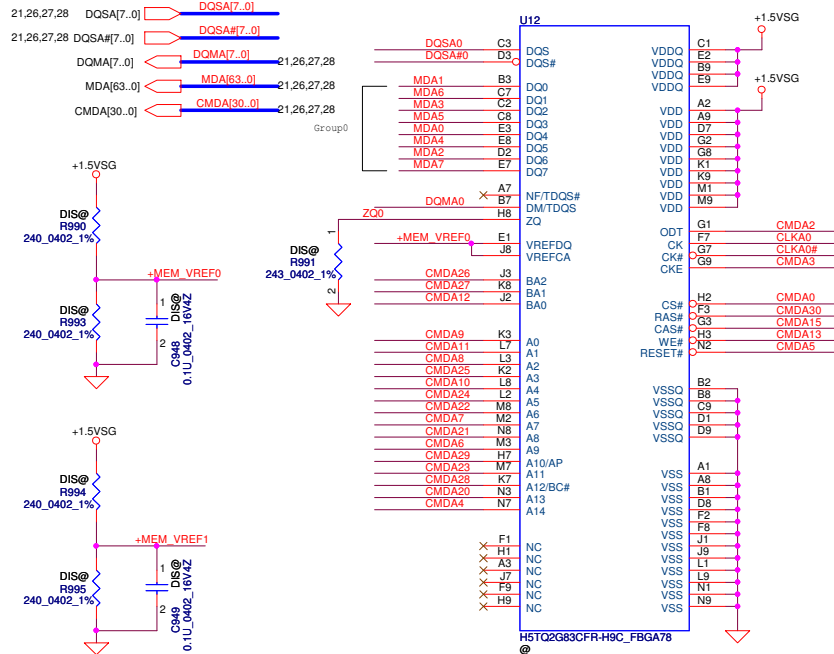




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# VRAM DDR3 chips

256Mx8 DDR3 \*8==>2GB



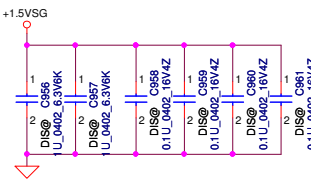
Command Bit	Default Pull-down
ODT#	10k
CKEx	10k
RST	10k
CS*	No Termination

Hynix : SA000054600 (S IC D3 256MX8/1333 H5TQ2G83CFR-H9C FBGA )

Elpida : SAxxxxxxx (S IC D3 256MX8/1333 xxxxxxxxxxxxxxxx )

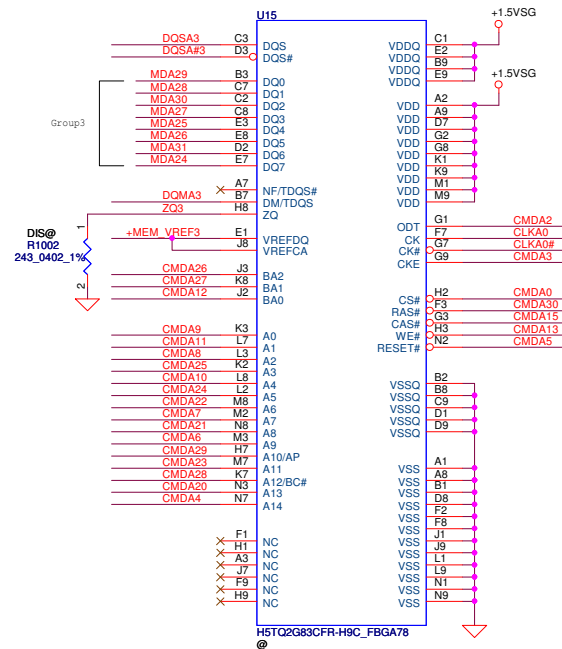
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

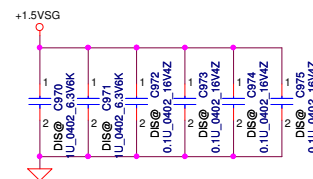


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Date: Monday, July 09, 2012		Sheet	25 of 58

**256Mx8 DDR3 \*8==>2GB**

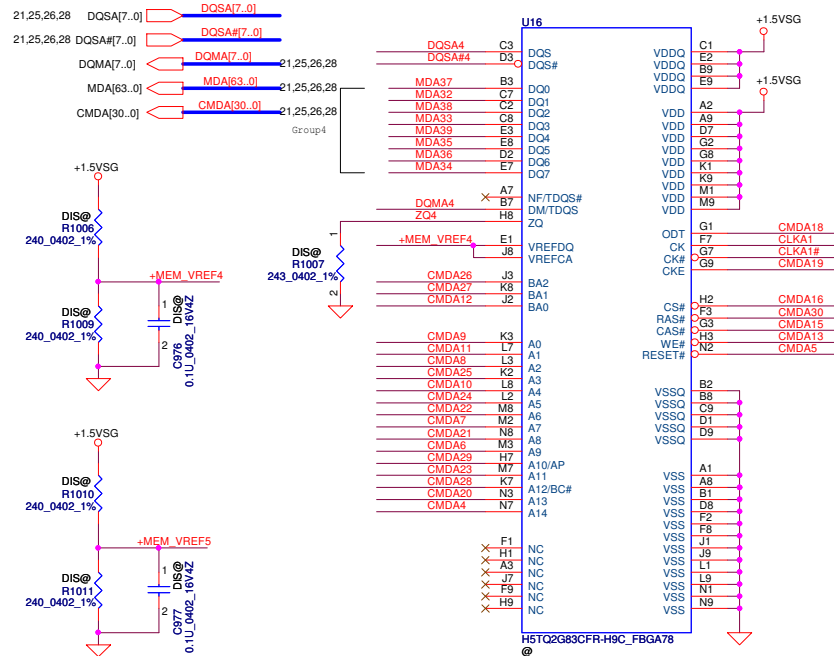


LOW HIGH

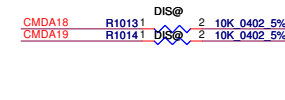
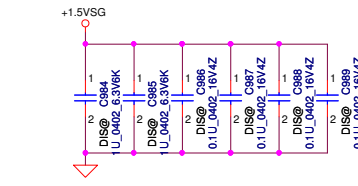
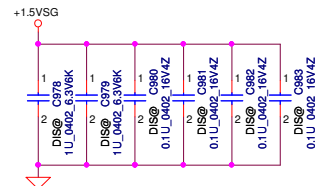
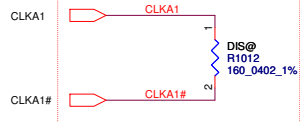


# VRAM DDR3 chips

256Mx8 DDR3 \*8==>2GB



place on 1st T trunk



Mode	D Address	0..31	32..63
CMD0	CS0_L#		
CMD1			
CMD2	ODT_L		
CMD3	CKE		
CMD4	A14	A14	
CMD5	RST	RST	
CMD6	A9	A9	
CMD7	A7	A7	
CMD8	A2	A2	
CMD9	A0	A0	
CMD10	A4	A4	
CMD11	A1	A1	
CMD12	BA0	BA0	
CMD13	WE*	WE*	
CMD14	A15	A15	
CMD15	CAS*	CAS*	
CMD16		CS0_H#	
CMD17			
CMD18		ODT_H	
CMD19		CKE_H	
CMD20	A13	A13	
CMD21	A8	A8	
CMD22	A6	A6	
CMD23	A11	A11	
CMD24	A5	A5	
CMD25	A3	A3	
CMD26	BA2	BA2	
CMD27	BA1	BA1	
CMD28	A12	A12	
CMD29	A10	A10	
CMD30	RAS*	RAS*	
Not Available			

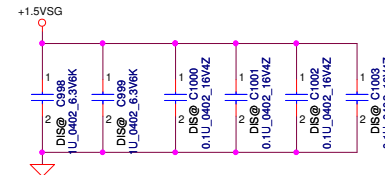
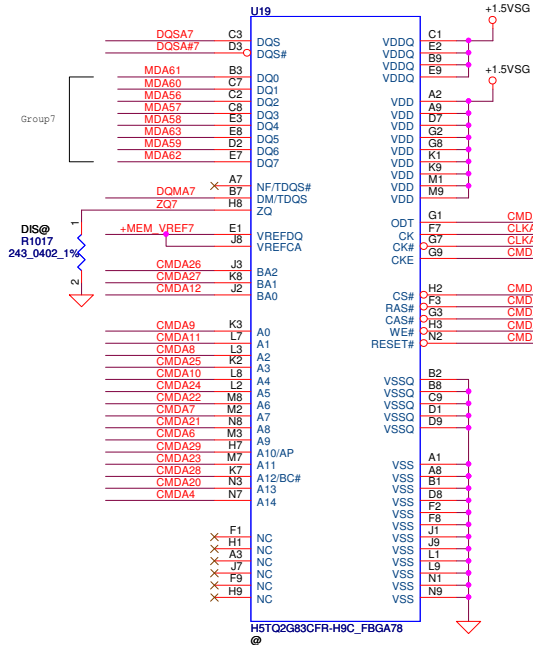
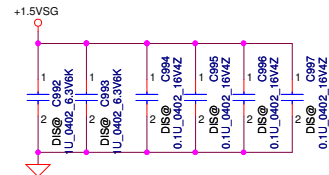
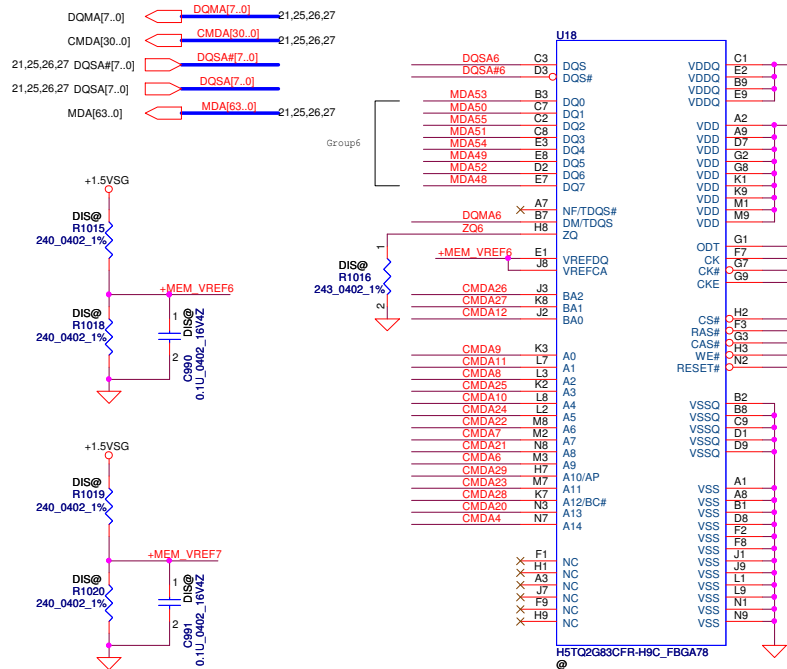
LOW HIGH

Hynix : SA000054600 (S IC D3 256MX8/1333 H5TQ2G83CFR-H9C FBGA )  
Elpida : SAxxxxxxxx (S IC D3 256MX8/1333 xxxxxxxxxxxxxxxxx )

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Sheet		27	of 58

# VRAM DDR3 chips

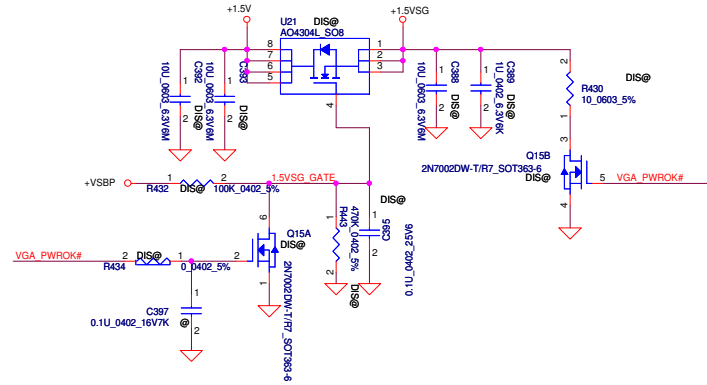
256Mx8 DDR3 \*8==>2GB



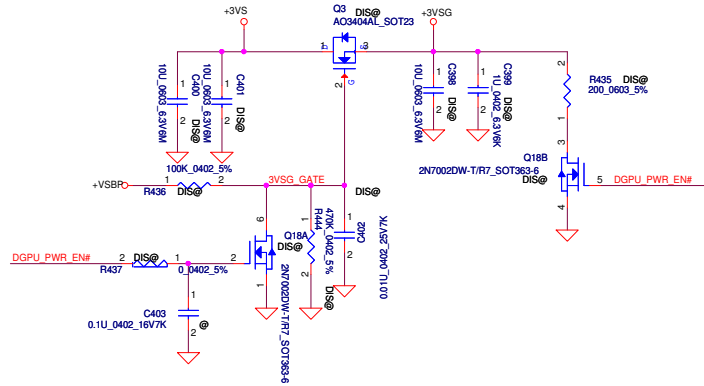
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

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				LA-8226P	1.0
				Date	Monday, July 09, 2012
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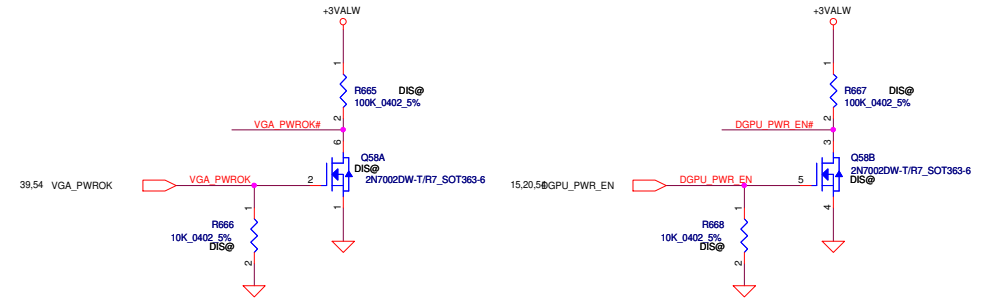
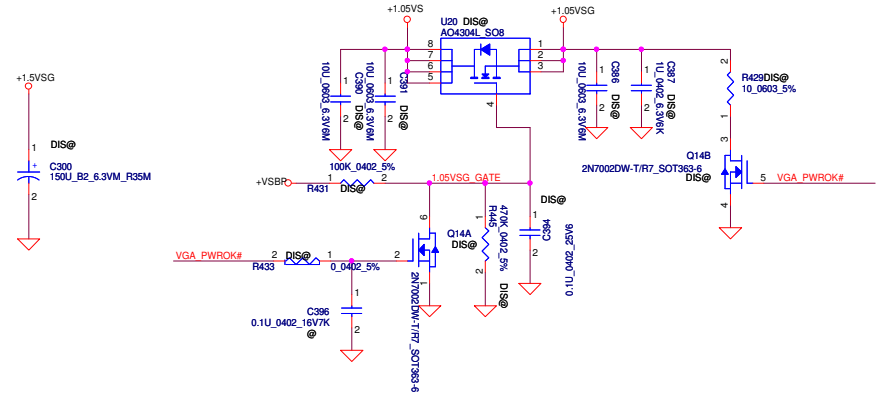
### +1.5V to +1.5VSG



### +3VS to +3VSG



### +VCCP to +1.05VSG



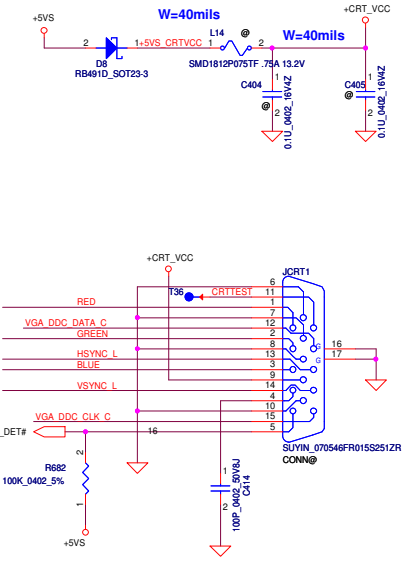
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/07/12	Deciphered Date	2012/12/31	PCH (2/8) PCIE, SMBUS, CLK		
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Date: Monday, July 09, 2012				Sheet 29 of 58		



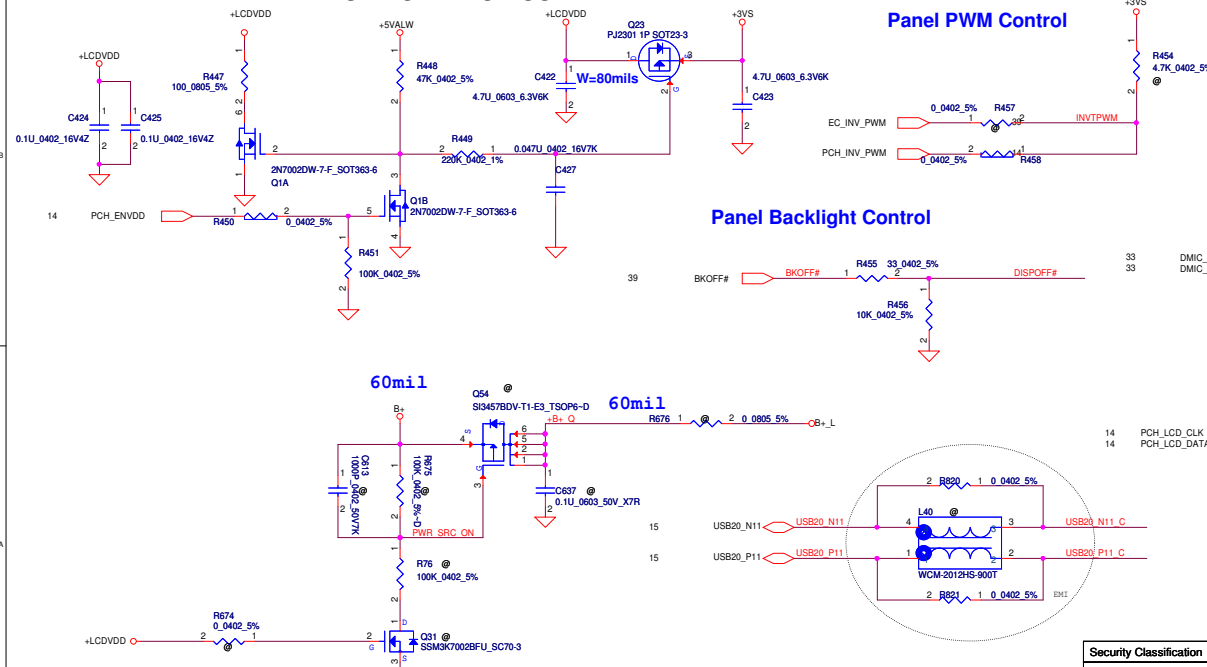
The diagram shows four timing diagrams for the L30ESDL5V0C3-2 C/A SOT-23 component. Each diagram shows two input signals connected to pins 2 and 3 of a component labeled D6, D7, D9, or D10. The signals are represented by horizontal lines with arrows indicating direction. The component is shown as a square with two pins and two internal arrows pointing towards each other.

- D6:** BLUE (pin 2) and GREEN (pin 3).
- D7:** RED (pin 2) and +CRT\_VCC (pin 3).
- D9:** HSYNC\_L (pin 2) and VSYNC\_L (pin 3).
- D10:** VGA\_DDC\_DATA\_C (pin 2) and VGA\_DDC\_CLK\_C (pin 3).

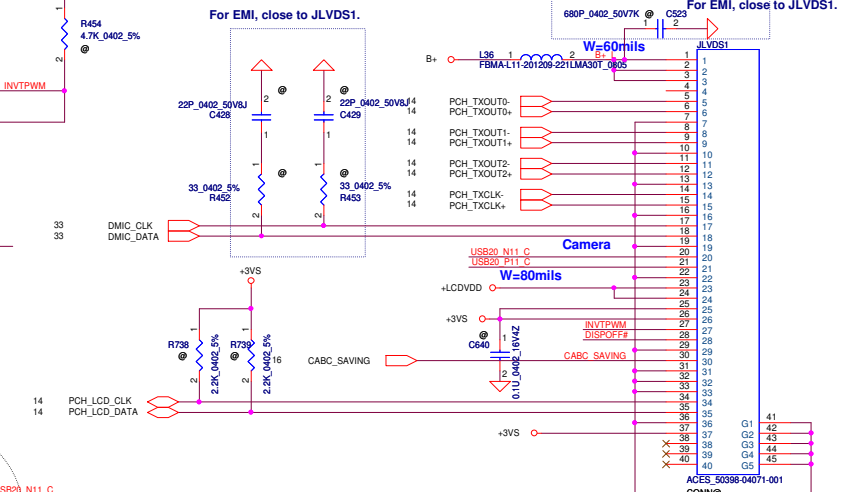
Each diagram is labeled with the component name L30ESDL5V0C3-2 C/A SOT-23 at the bottom.



### Panel PWM Control

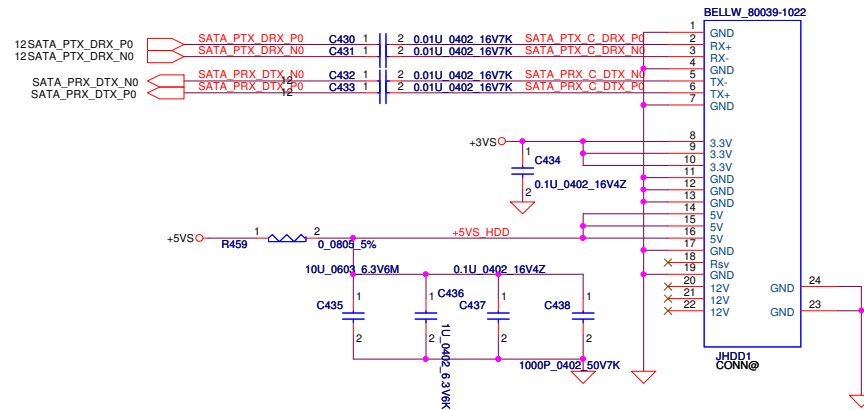


## Panel Backlight Control

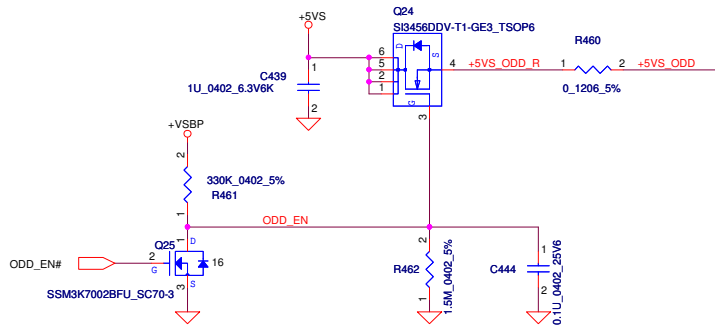


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				Document Number <b>LA-8226P</b>
Date: Monday, July 09, 2012				Rev 1.0 Sheet 30 of 58

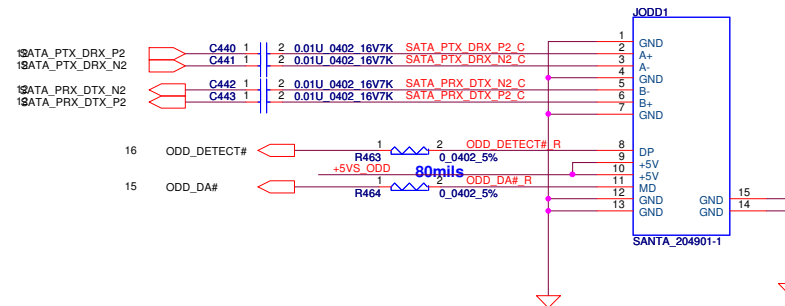
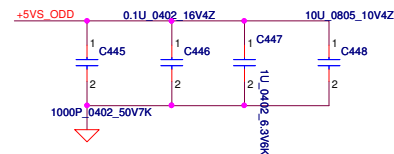
## SATA HDD Conn.



## SATA ODD Conn.

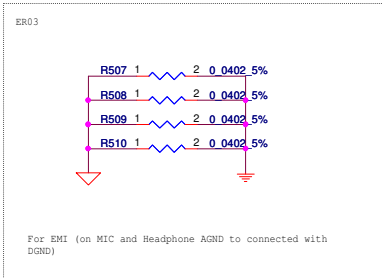
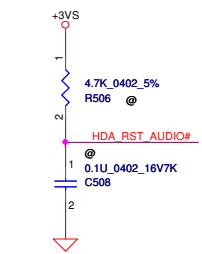
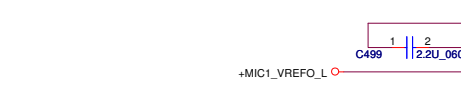
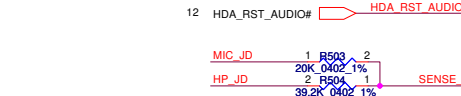
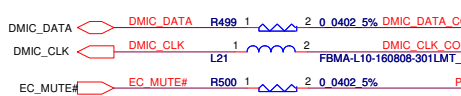
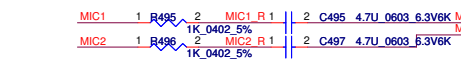
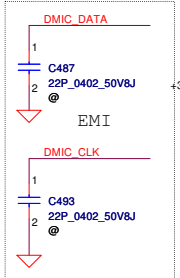


Place caps. near ODD CONN.

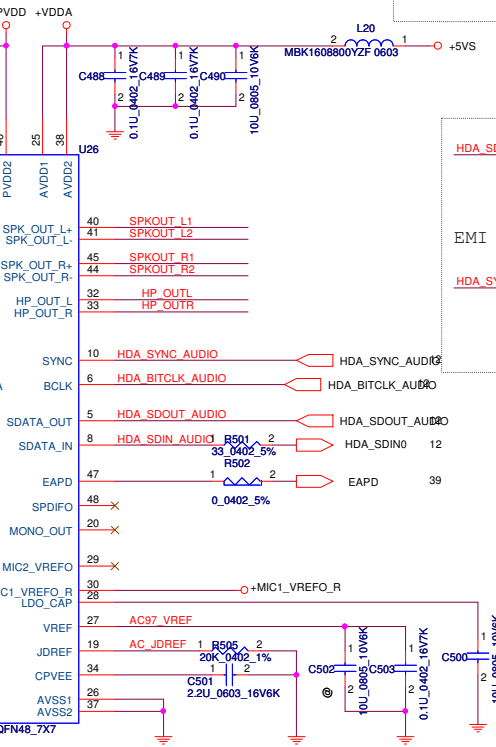
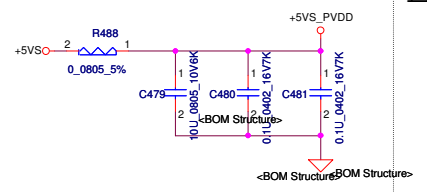


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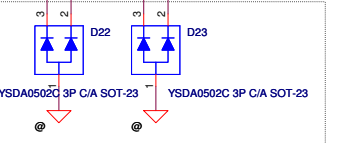
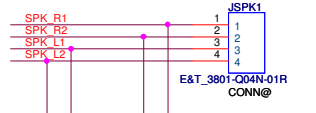
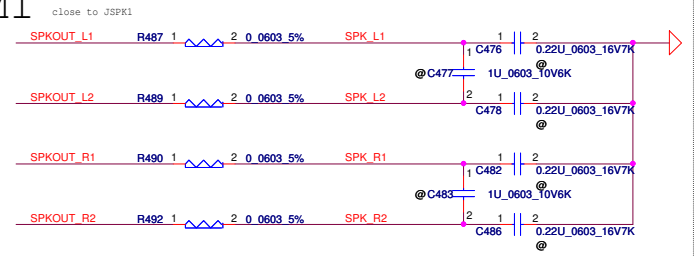




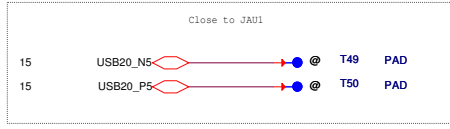
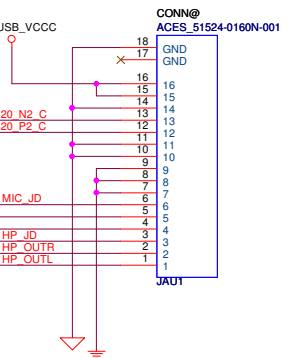
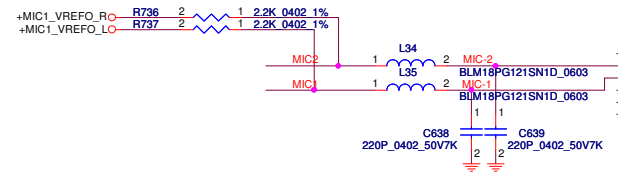
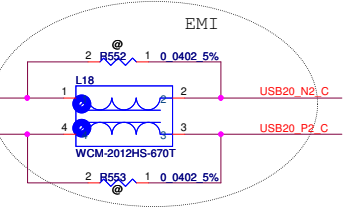
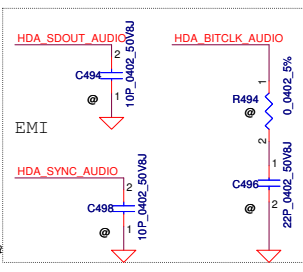
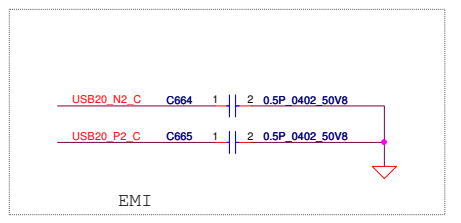
For EMI (on MIC and Headphone AGND to be connected with GND)



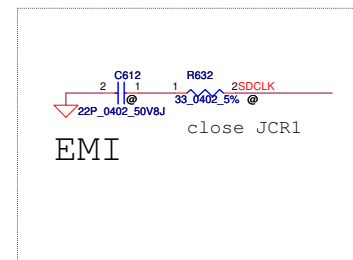
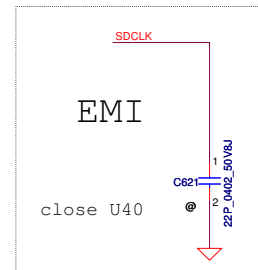
# EMI



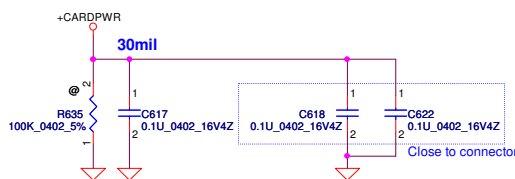
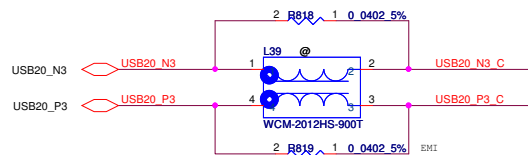
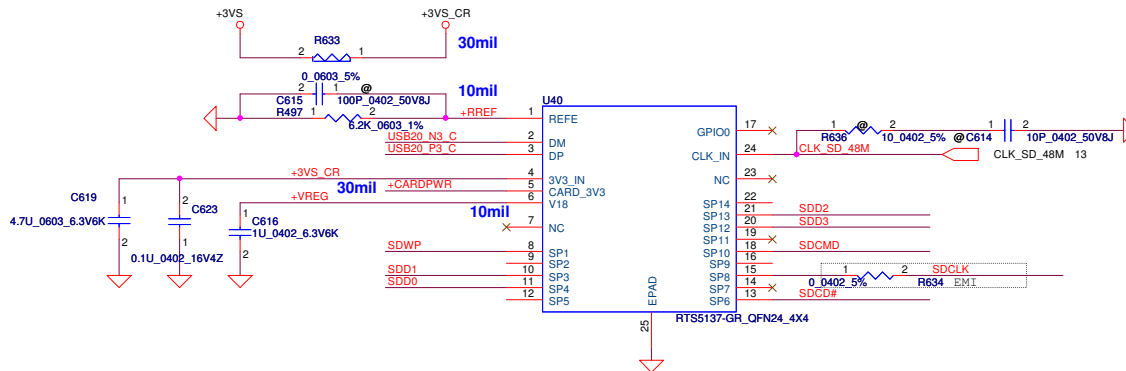
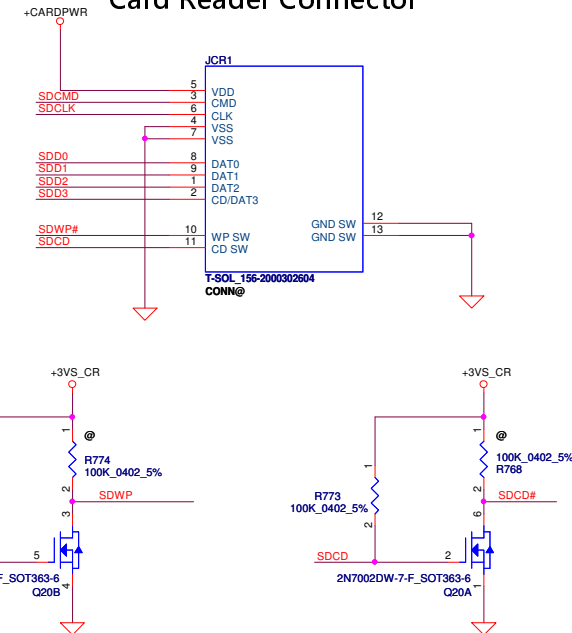
# ESD



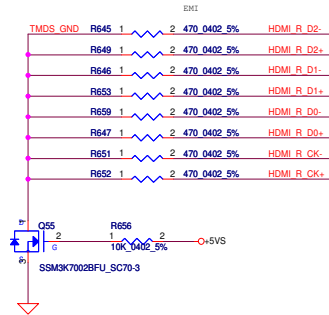
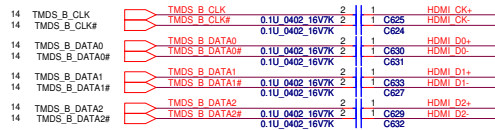
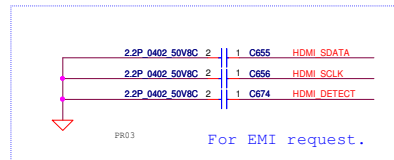
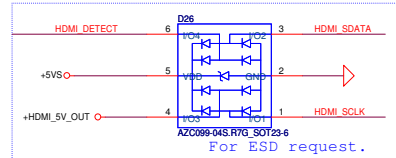
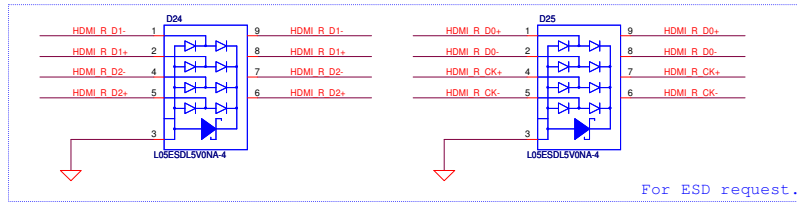
Security Classification		Compal Secret Data				Compal Electronics, Inc.											
Issued Date		2011/07/12		Deciphered Date		2012/12/31		Title		HD CODEC ALC269							
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										Document Number		LA-8226P					
										Date:		Monday, July 09, 2012		Sheet		33 of 58	
										Rev							



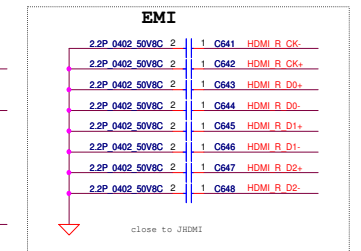
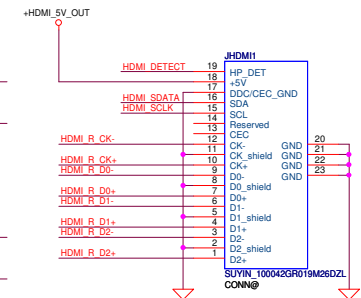
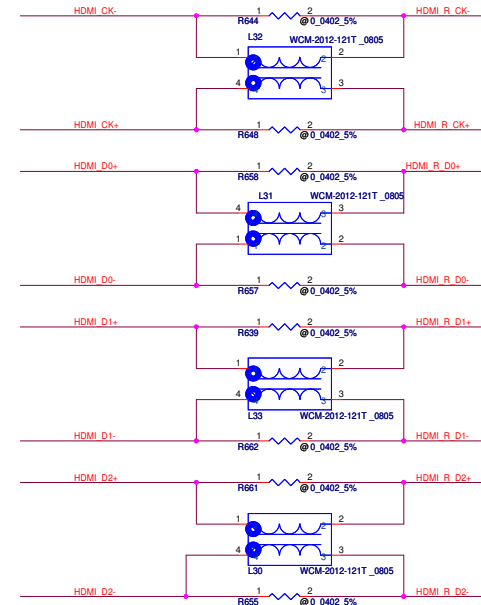
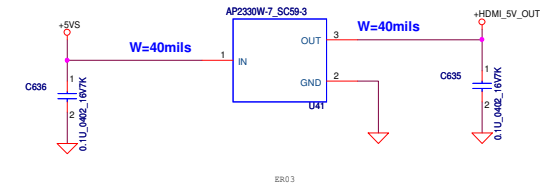
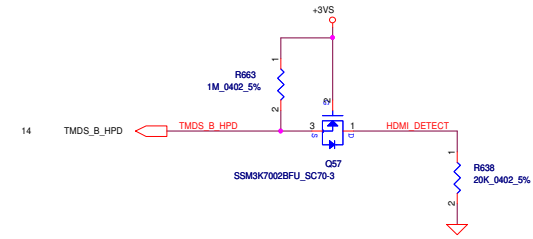
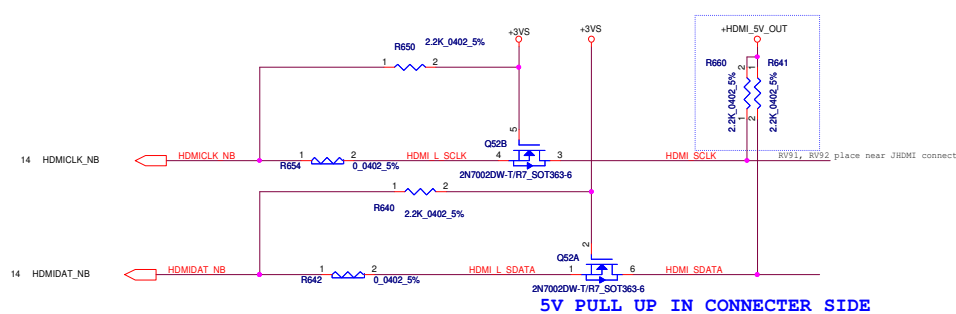
## Card Reader Connector



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HDMI



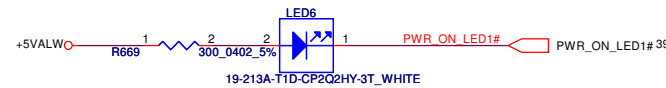
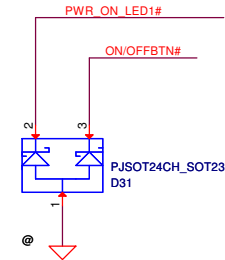
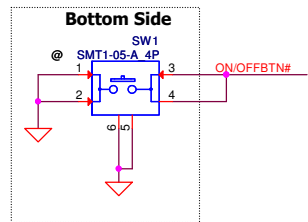
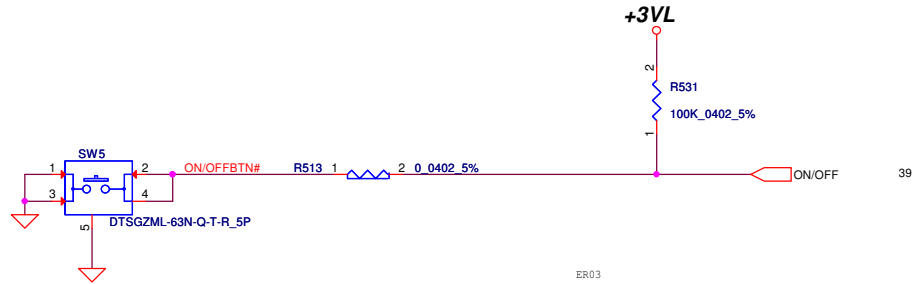
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		HDMI Connector	
2011/07/12		2012/12/31		Document Number	
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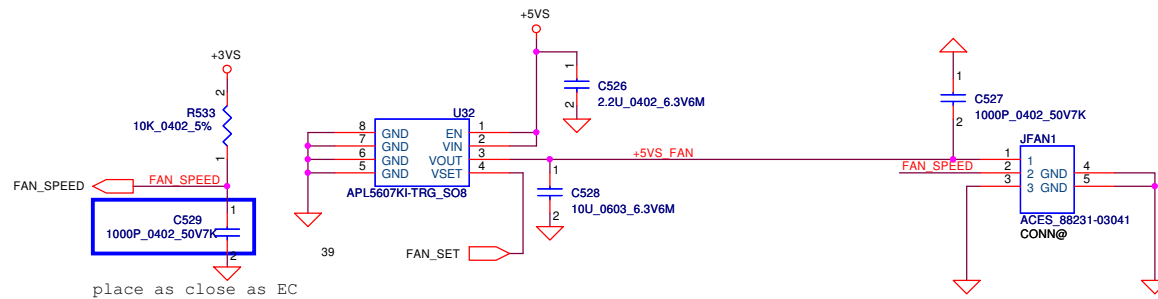


## Power Button

ON/OFF switch



## Fan Control Circuit

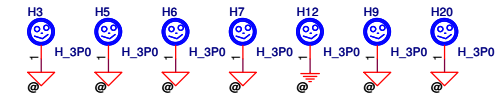


## Screw Hole

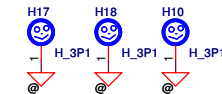
## 2.7



### 3.0



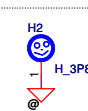
### 3.1



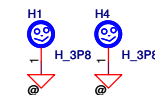
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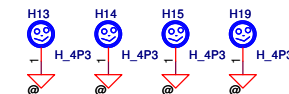
## 3.8



### 3.8

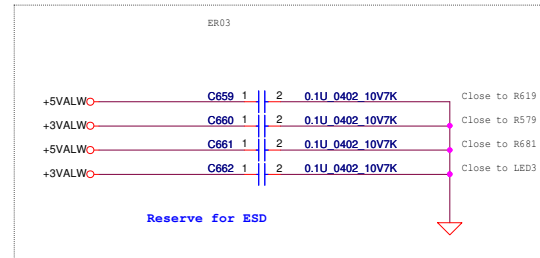
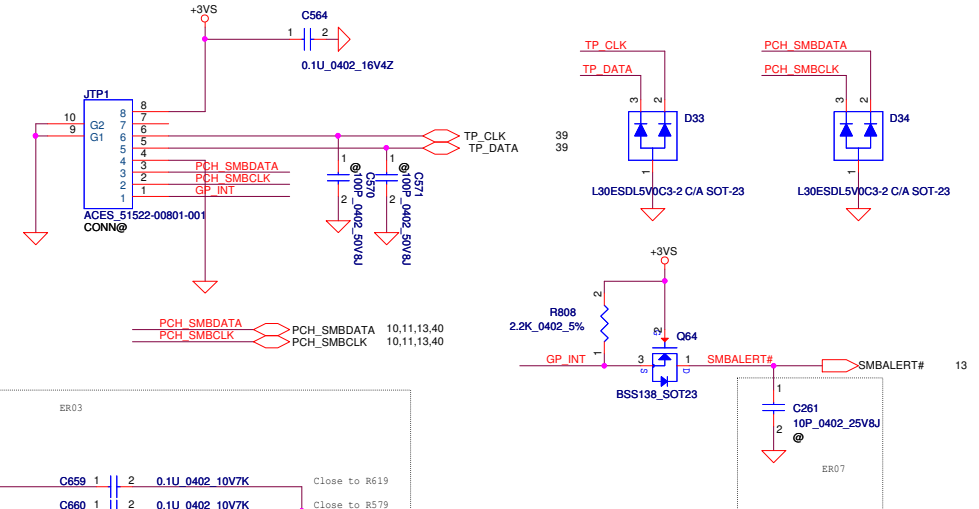
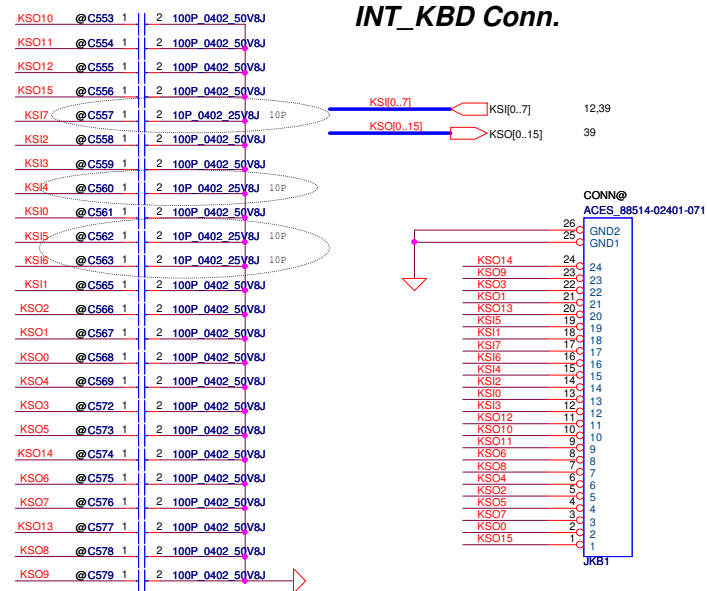


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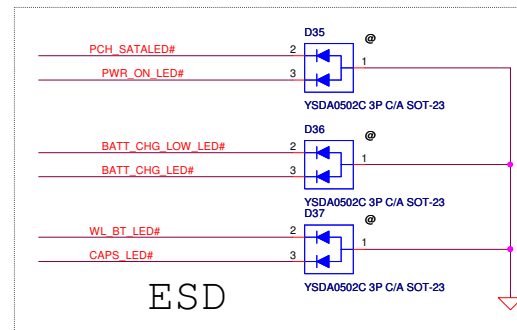
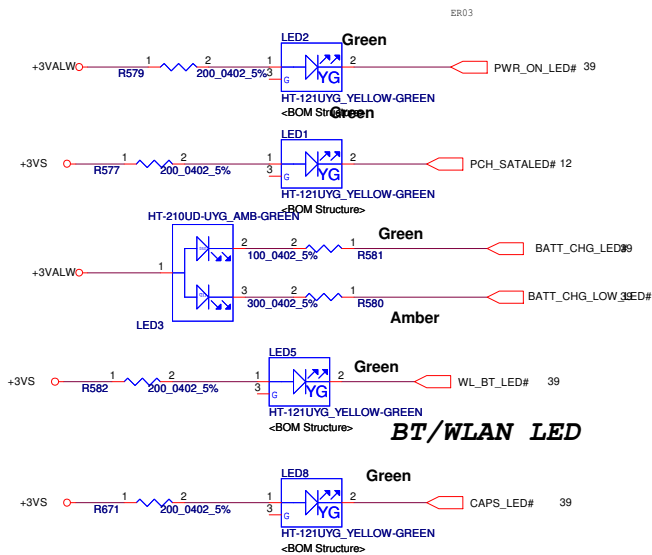


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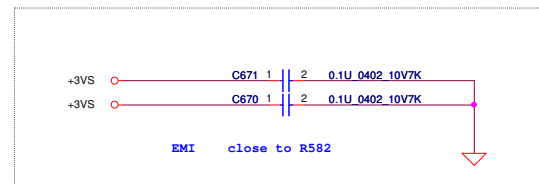
## Touch/B Connector



**LED**

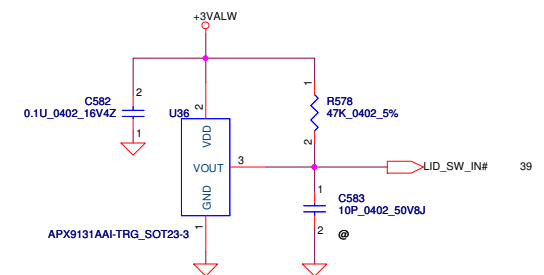


## ESD

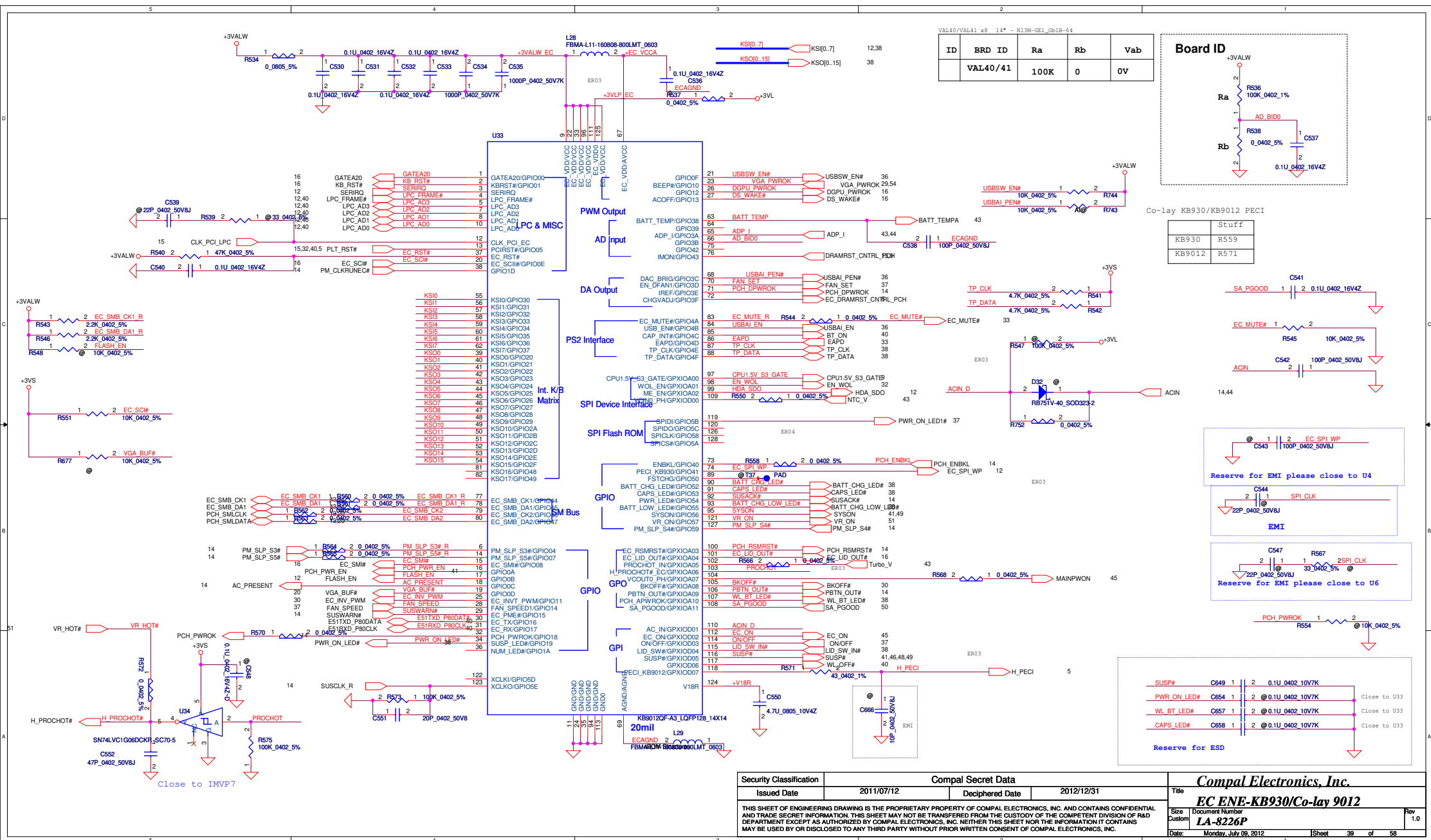


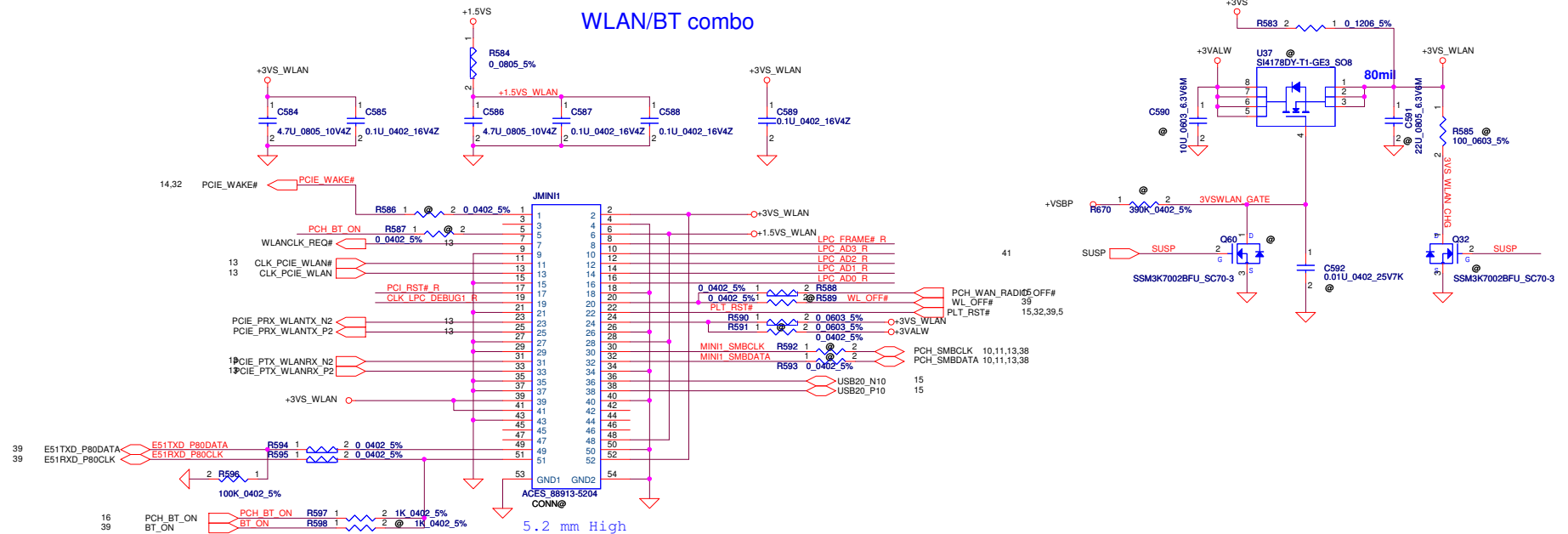
### Lid Switch

(Hall Effect Switch)



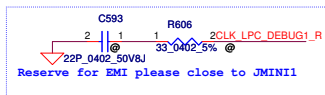
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	KB/EC ROM/TP/FUN/LED	
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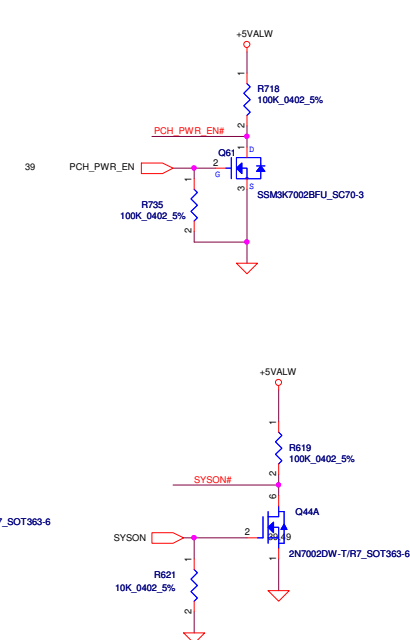
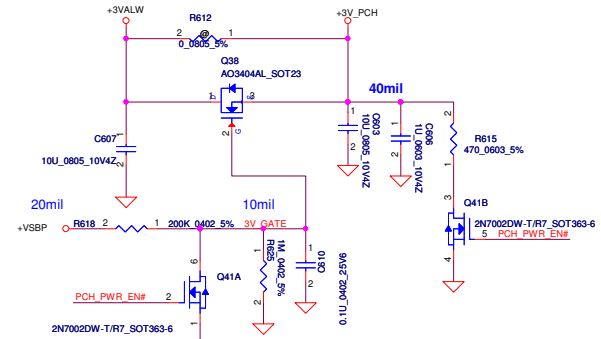
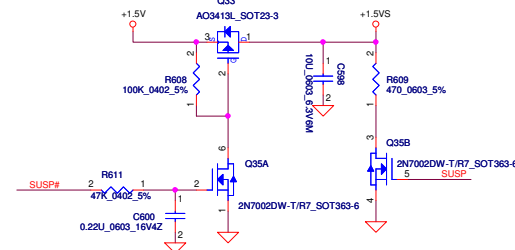
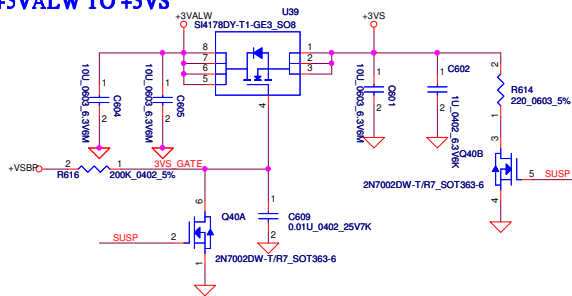


Reserve for SW mini-pcie debug card.  
Series resistors closed to KBC side.

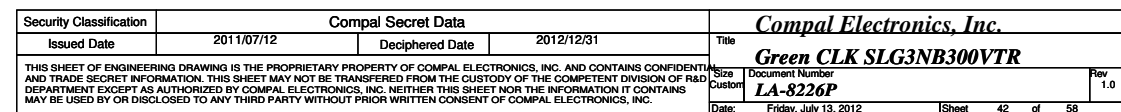
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LPC_AD3 R	R600	1	2	0.0402 5%	LPC_AD3	12.39
LPC_AD2 R	R601	1	2	0.0402 5%	LPC_AD2	12.39
LPC_AD1 R	R602	1	2	0.0402 5%	LPC_AD1	12.39
LPC_AD0 R	R603	1	2	0.0402 5%	LPC_AD0	12.39
PLT_RST# R	R604	1	2	0.0402 5%	PLT_RST#	12.39
CLK_LPC_DEBUG1 R	R605	1	2	0.0402 5%	CLK_LPC_DEBUG1	12.39



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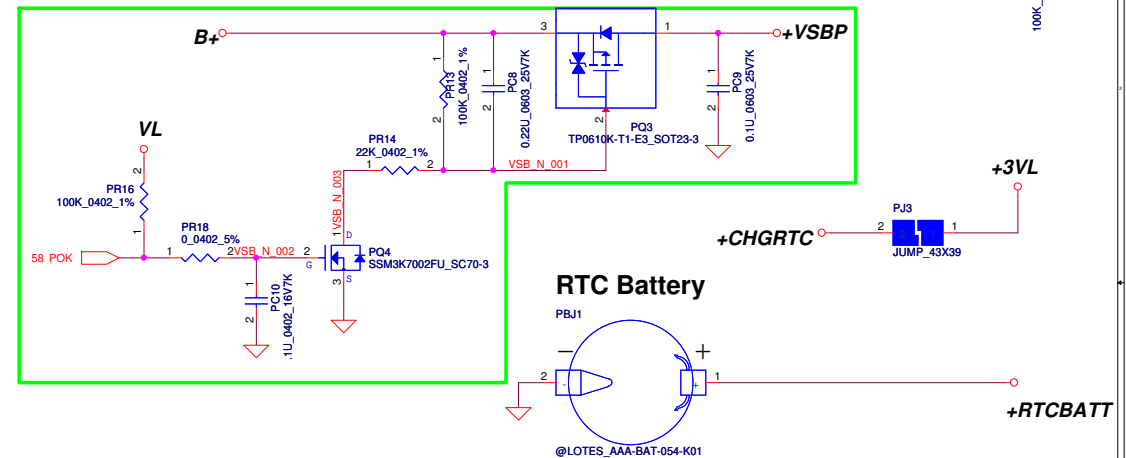
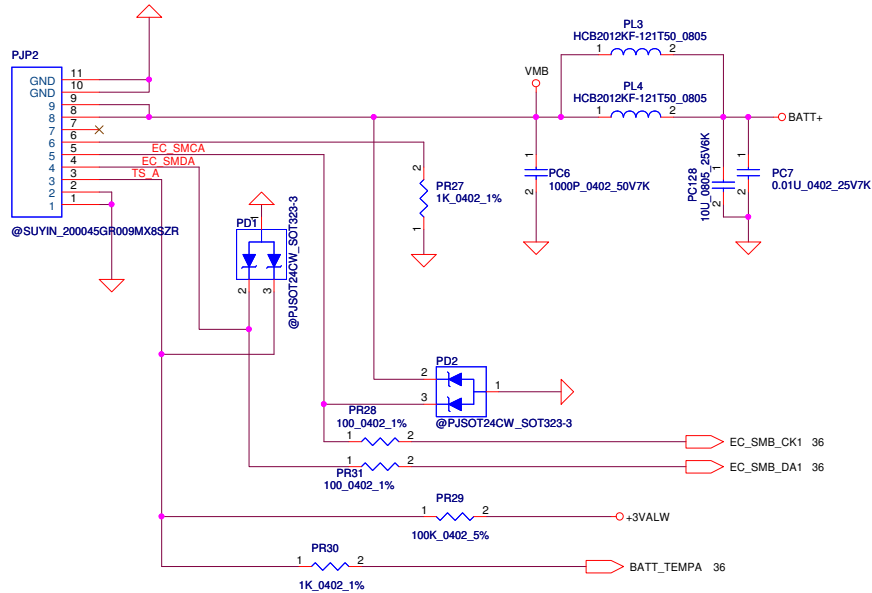
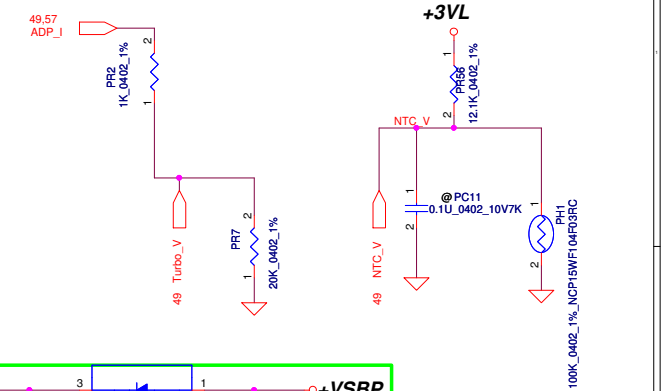
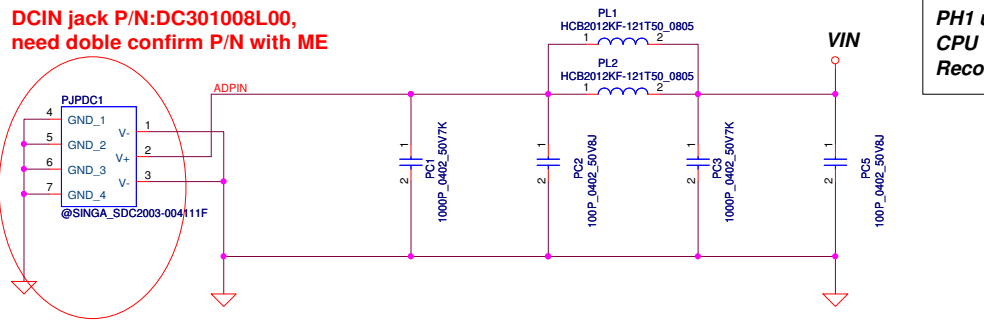
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**DCIN jack P/N:DC301008L00,  
need doble confirm P/N with ME**

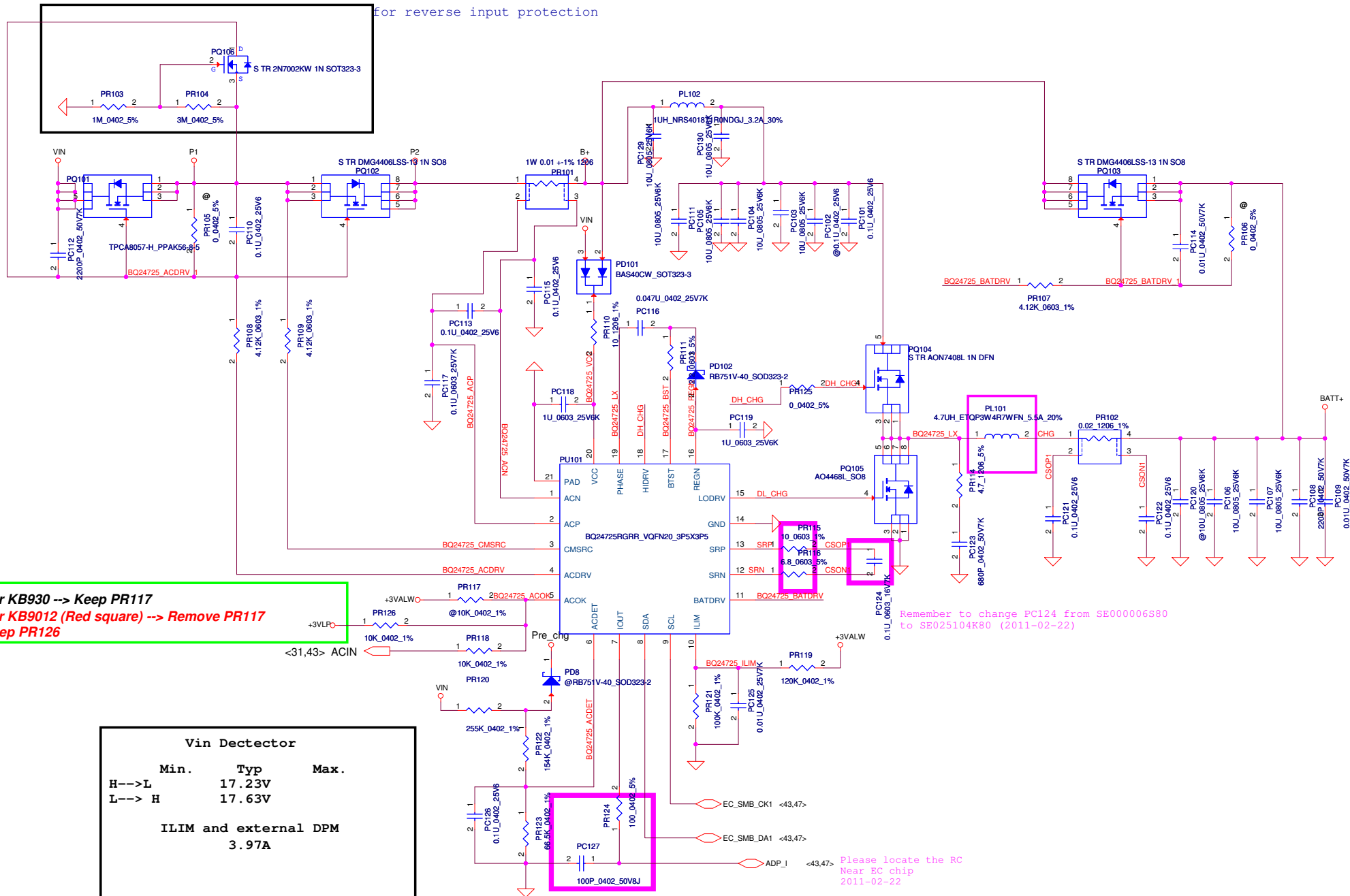
PH1 under CPU botten side :  
CPU thermal protection at 93 +-3 degree C  
Recovery at 56 +-3 degree C



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For reverse input protection



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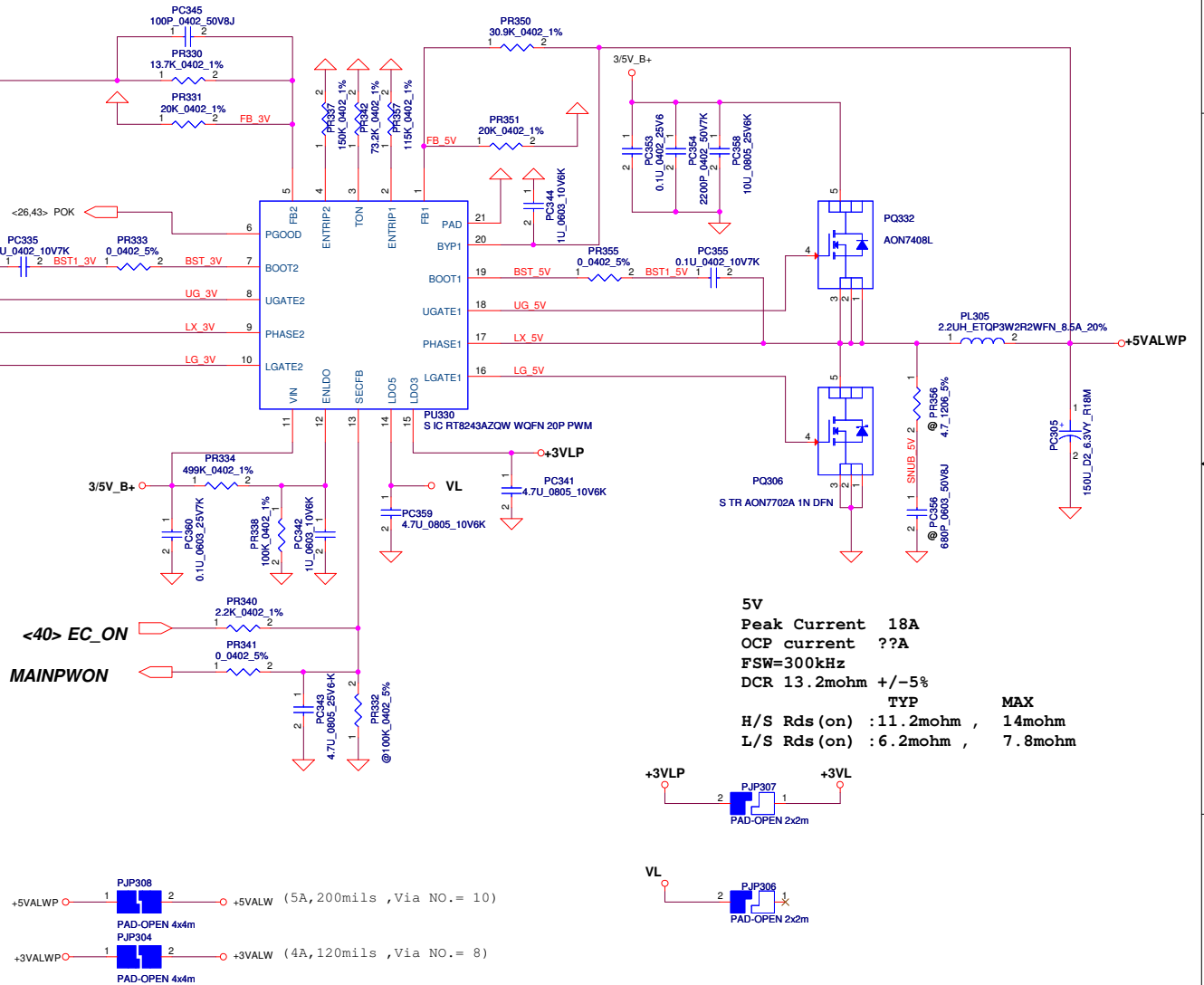
3.3V  
Peak Current 18A  
OCP current ??A  
FSW=300kHz  
DCR 38mohm +/-5%

	TYP	MAX
H/S Rds (on)	:11.2mohm	14mohm
L/S Rds (on)	:6.2mohm	7.8mohm

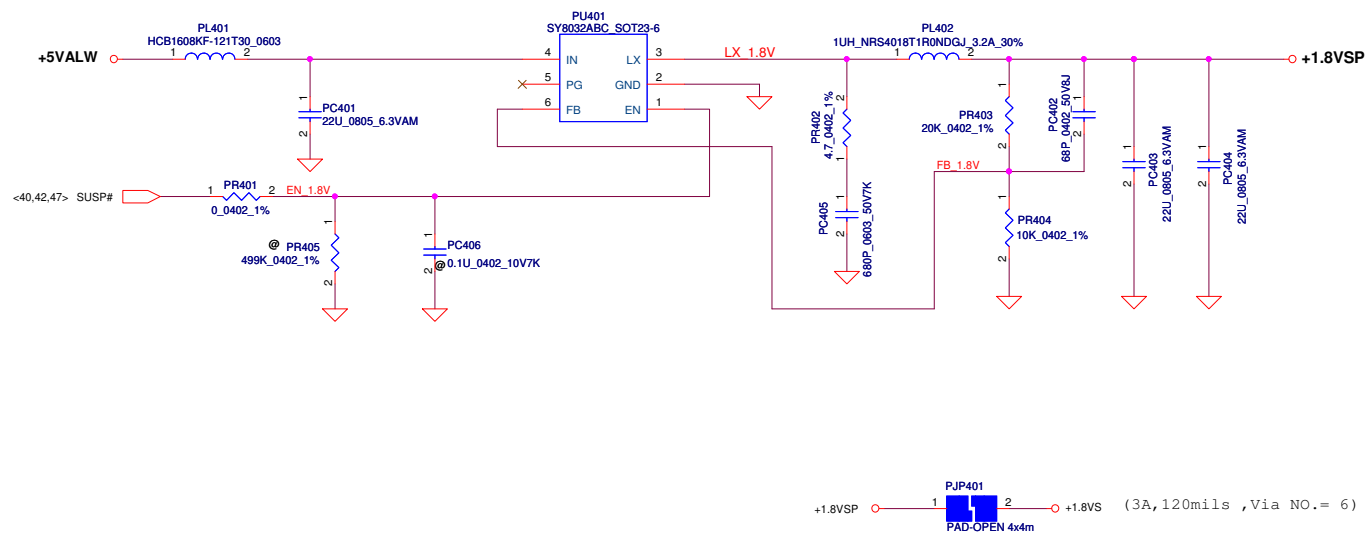
<40> EC\_ON  
<40> MAINPWON

5V  
Peak Current 18A  
OCP current ??A  
FSW=300kHz  
DCR 13.2mohm +/-5%

	TYP	MAX
H/S Rds (on)	:11.2mohm	14mohm
L/S Rds (on)	:6.2mohm	7.8mohm



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				Document Number		Rev	
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				Date:		Monday, July 09, 2012	



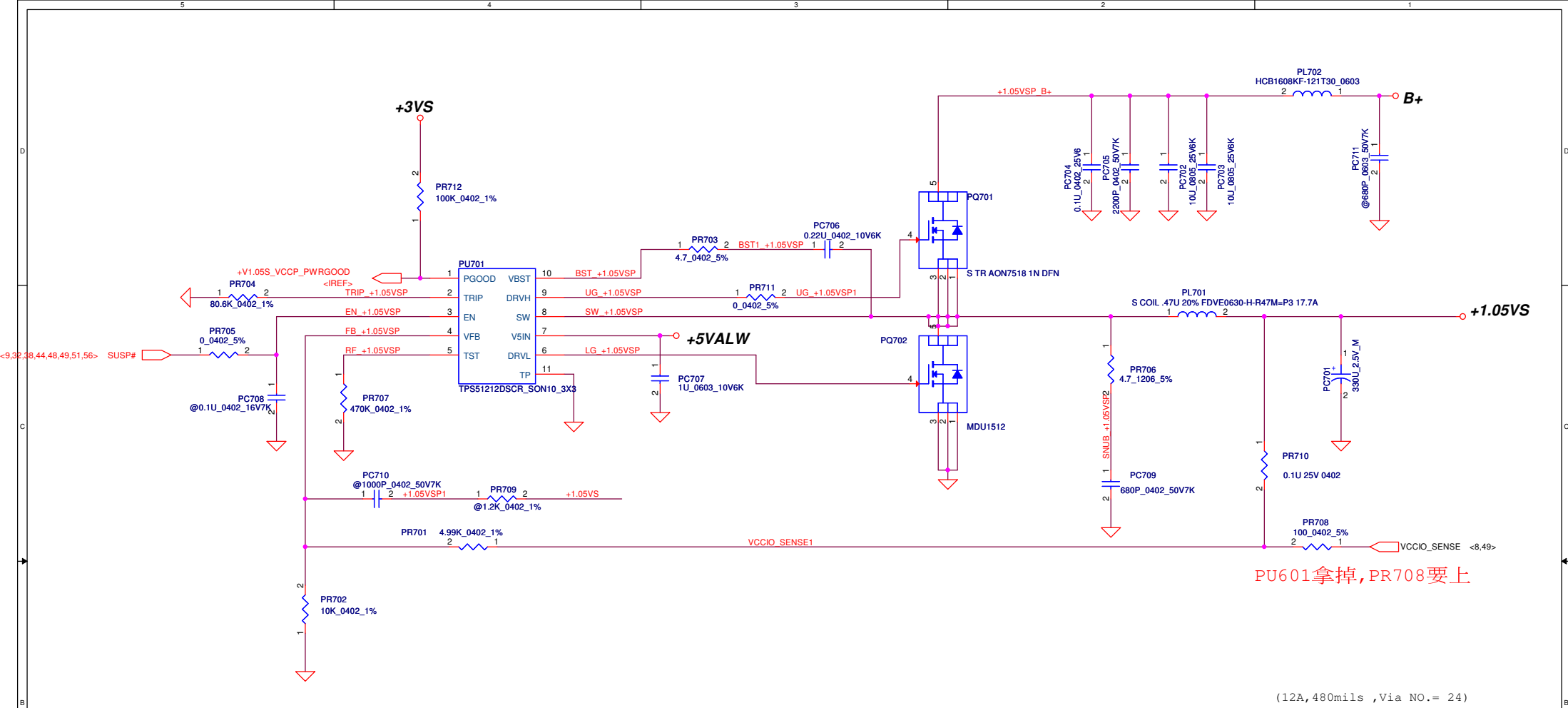
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Issued Date	2009/01/23	Deciphered Date	2012/12/31	PWR-1.8VSP	
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(8.5A,360mils ,Via NO.= 17)

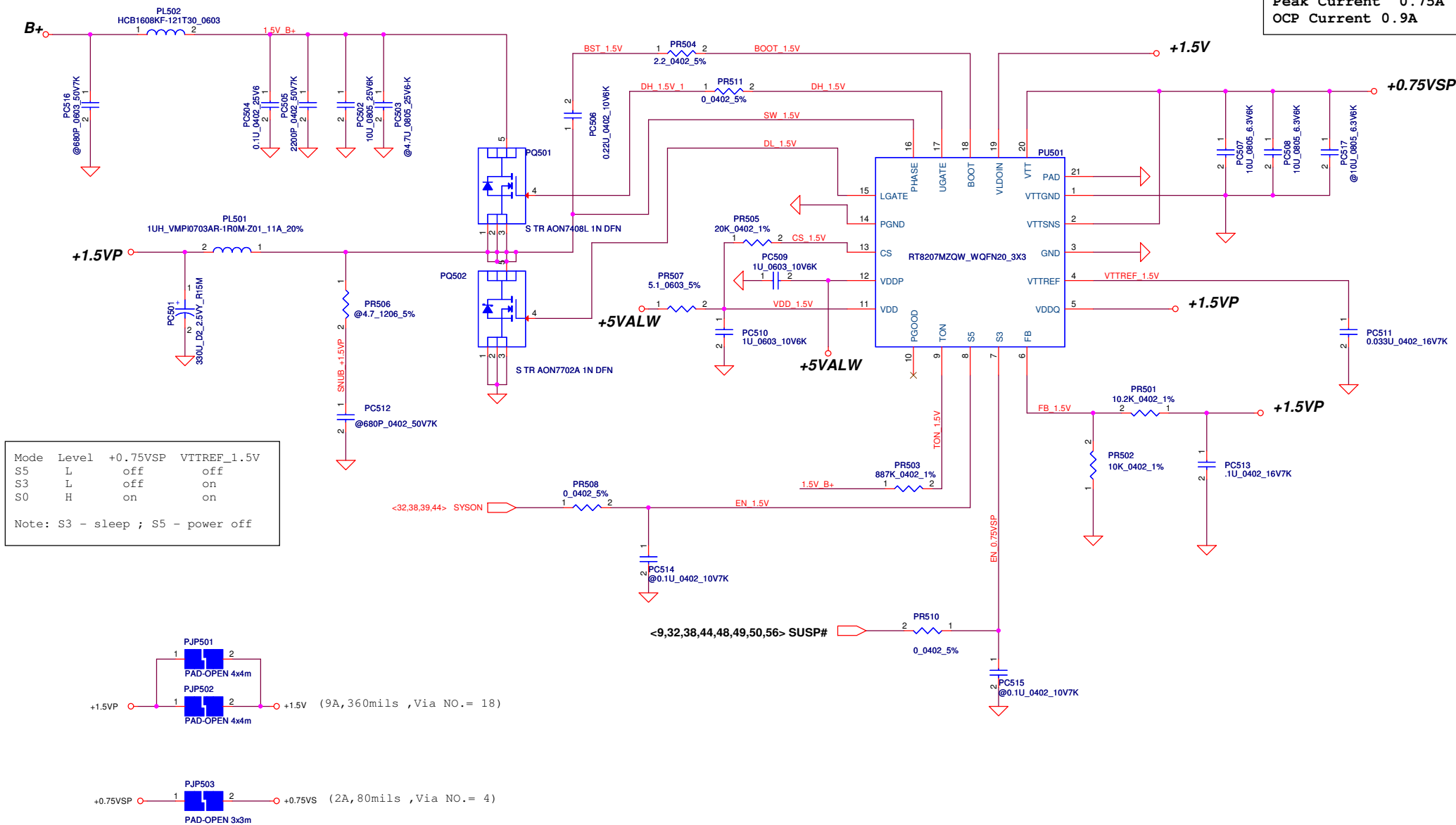
PJP606,PJP607先斷開,確定拿掉PU605再接上

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								PWR-V1.05SP			
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0.75Volt +/- 5%  
TDC 0.525A  
Peak Current 0.75A  
OCP Current 0.9A

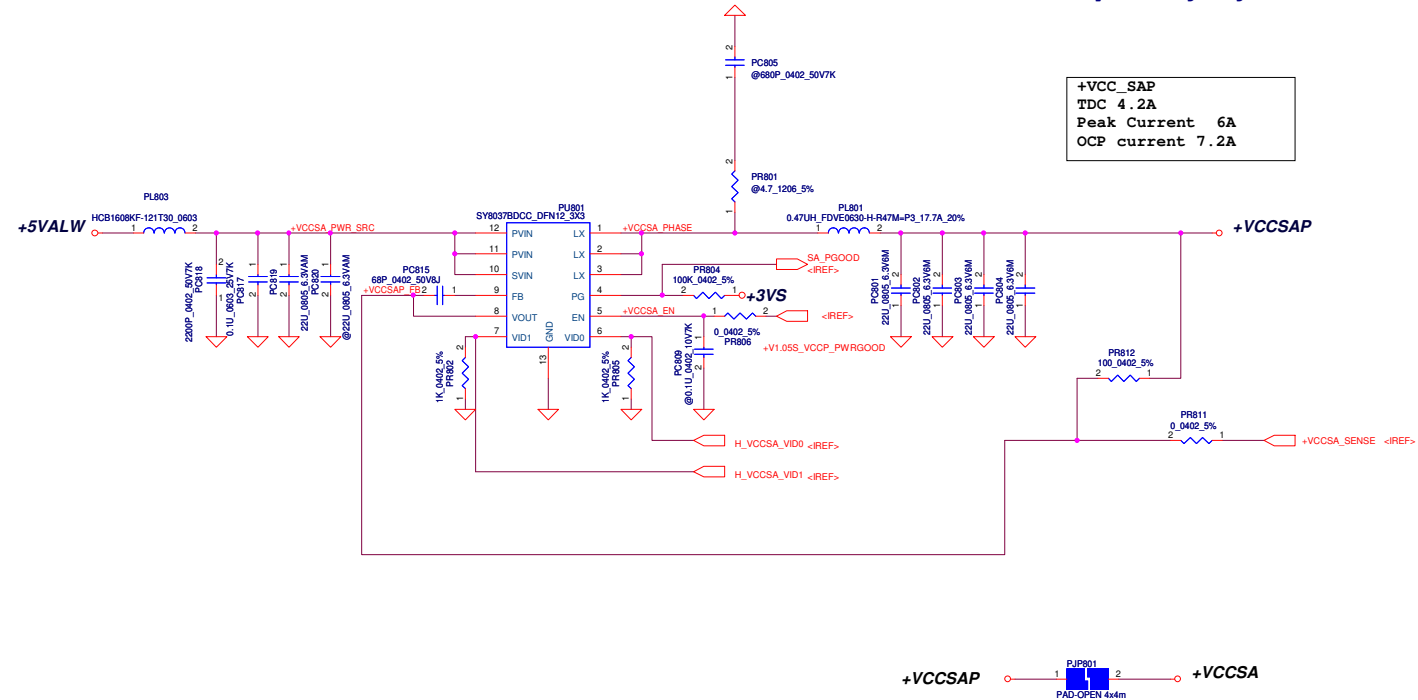


**The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.**

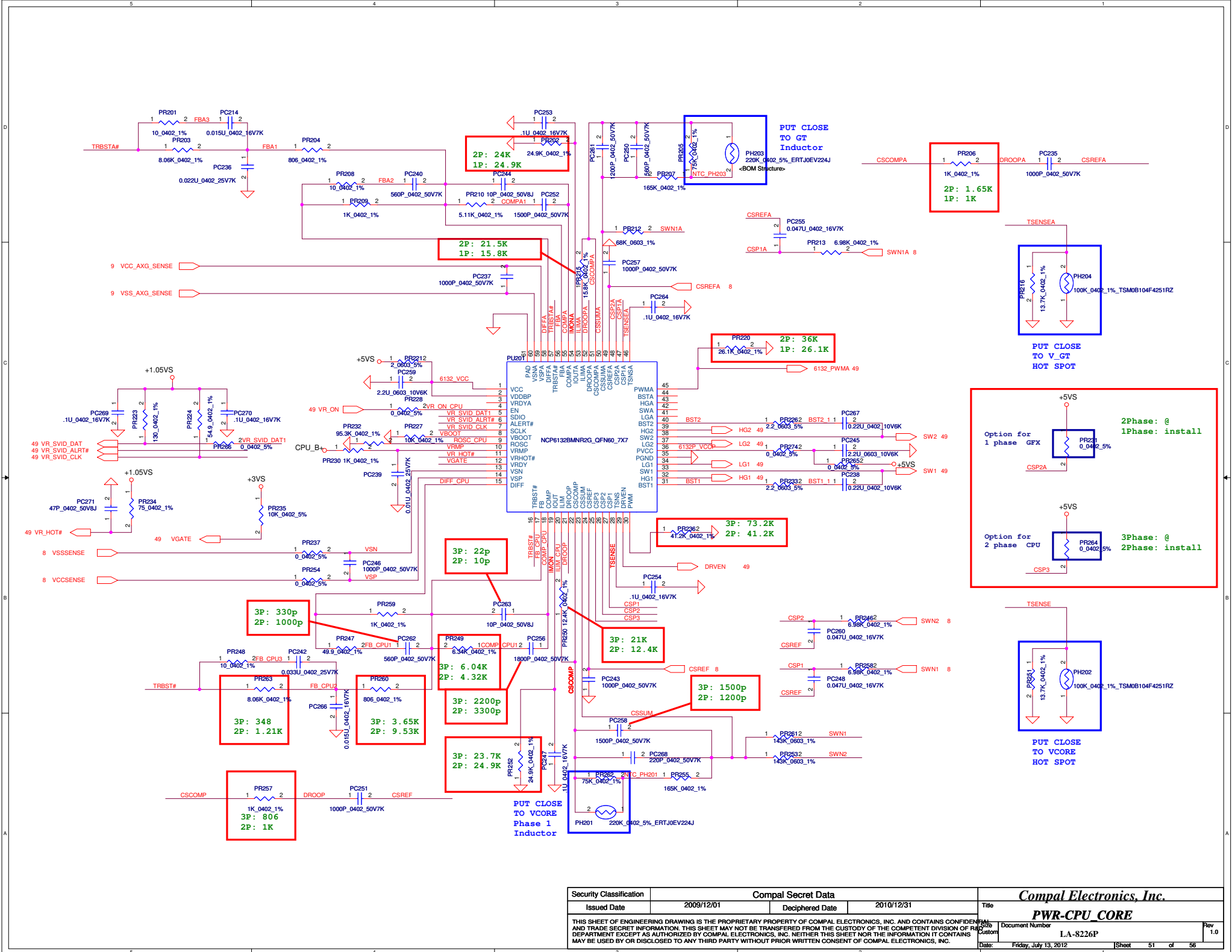
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

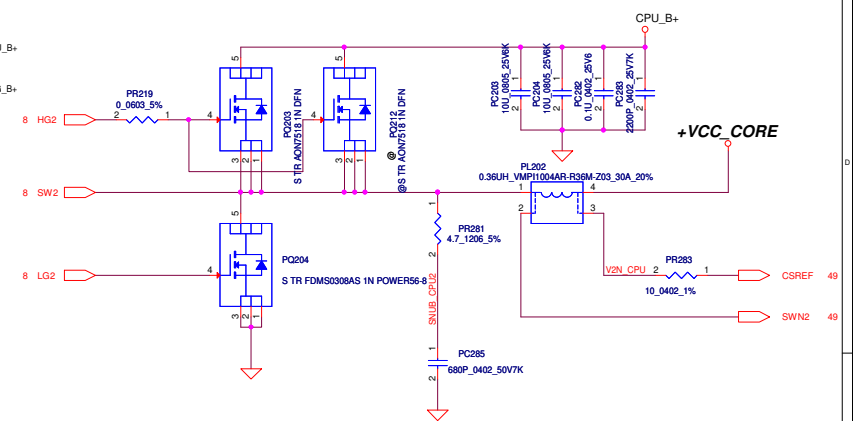
```
+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A
```





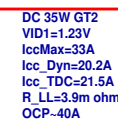


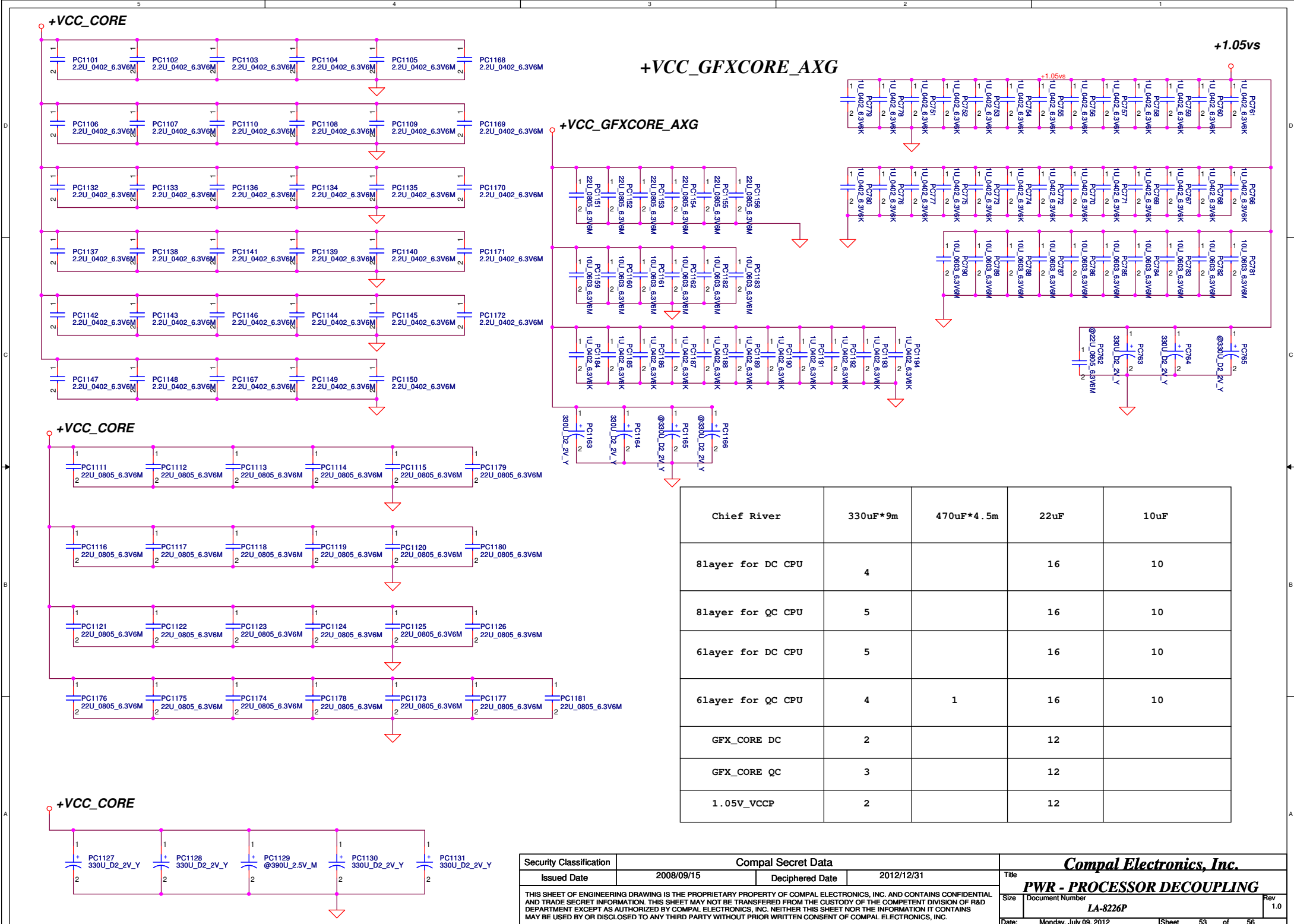
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2010/12/31	Title	PWR-CPU_CORE
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DC 35W CPU  
VID1=1.05V  
IccMax=53A  
Icc\_Dyn=43A  
Icc\_TDC=33A  
R\_LL=1.9m ohm  
OCP~65A

```
DC 35W CPU
solution: 2+1
MOS: cpu_core --> 上1(CSD17308) 下1(TPCA8059)
      Gfx_core --> 上1(CSD17308) 下1(TPCA8057)
```





**+VCC\_GFXCORE\_AXG**

+1.05vs

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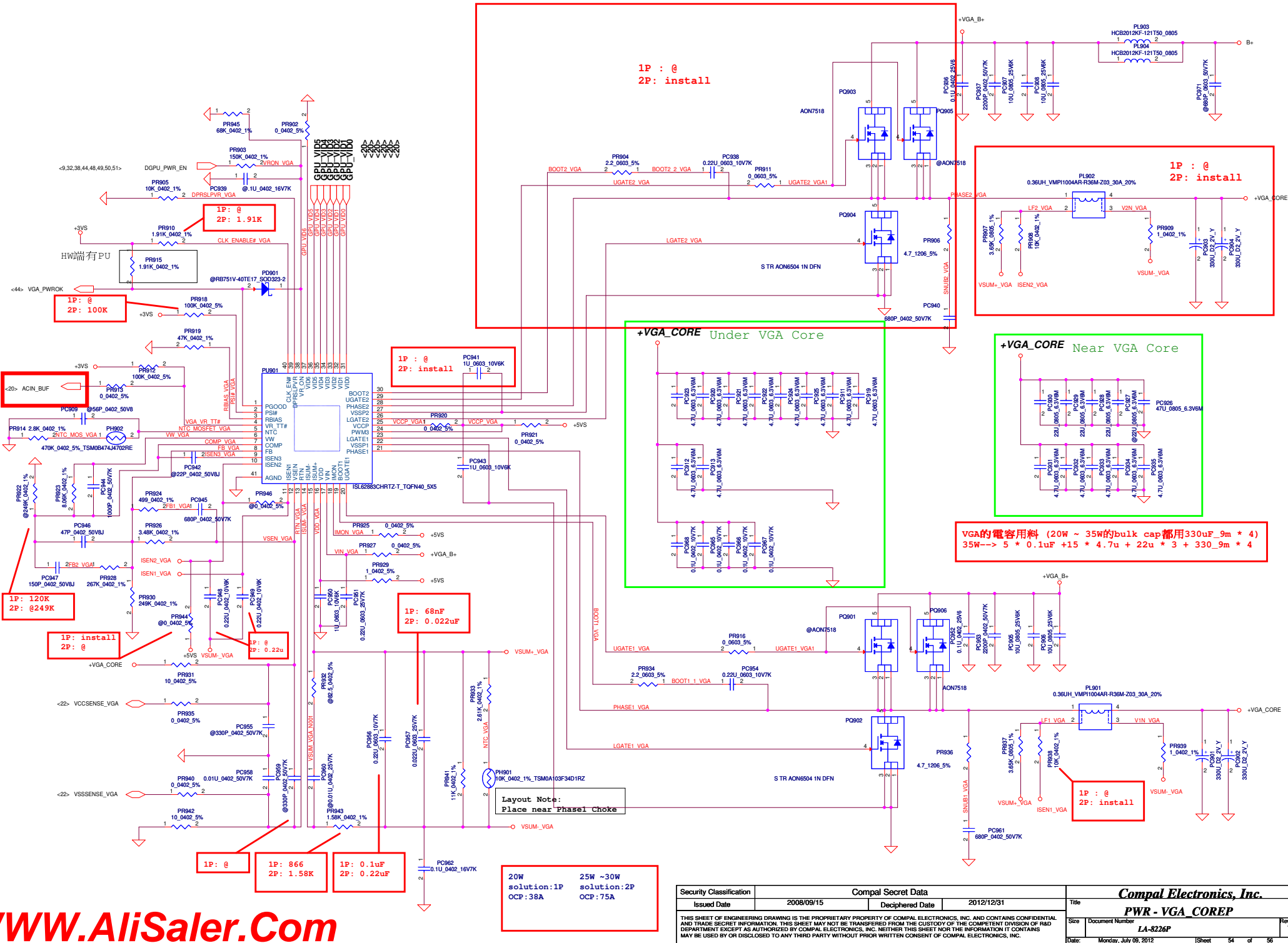
**PWR - PROCESSOR DECOUPLING**

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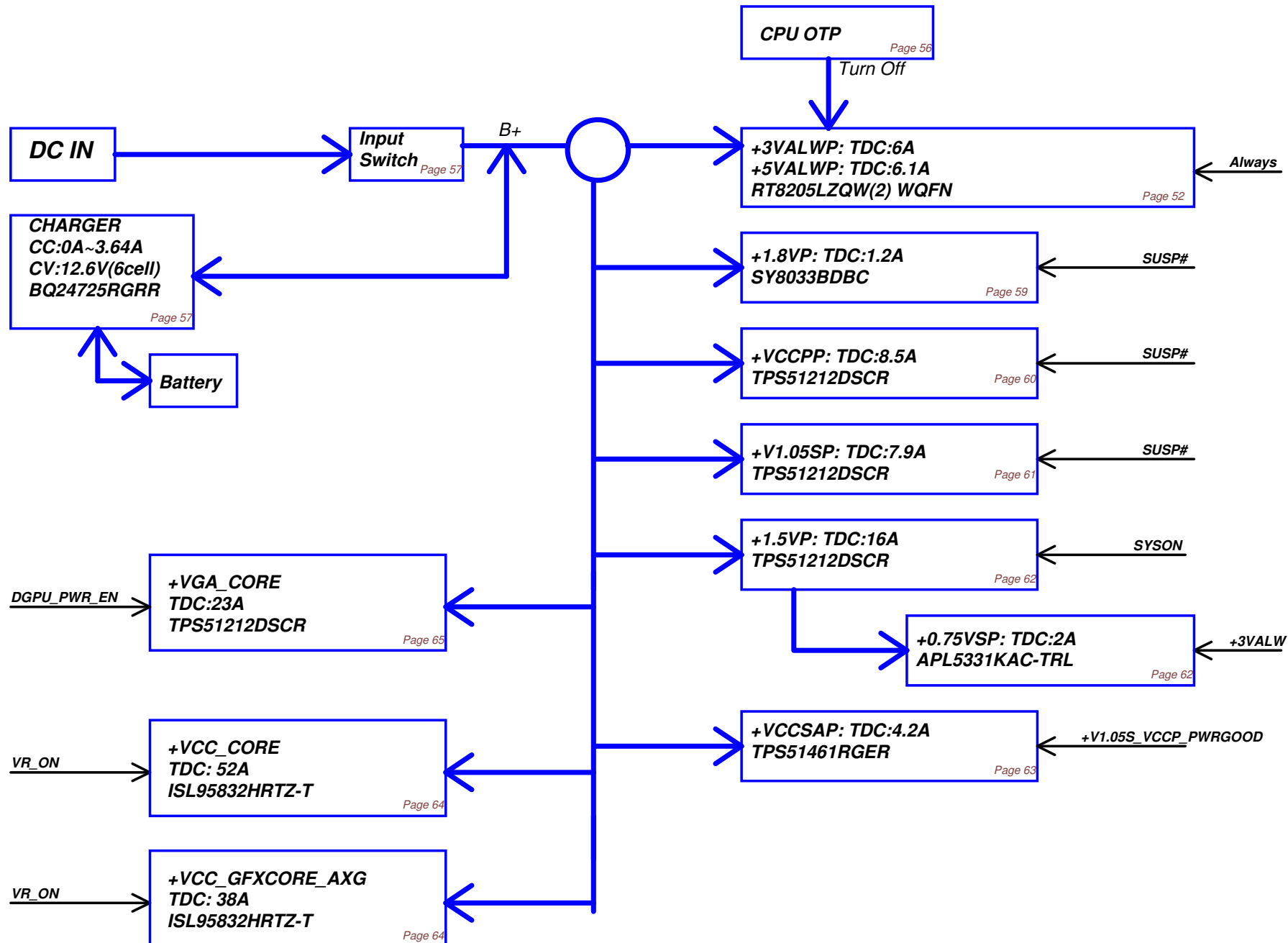
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Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	



# Power block

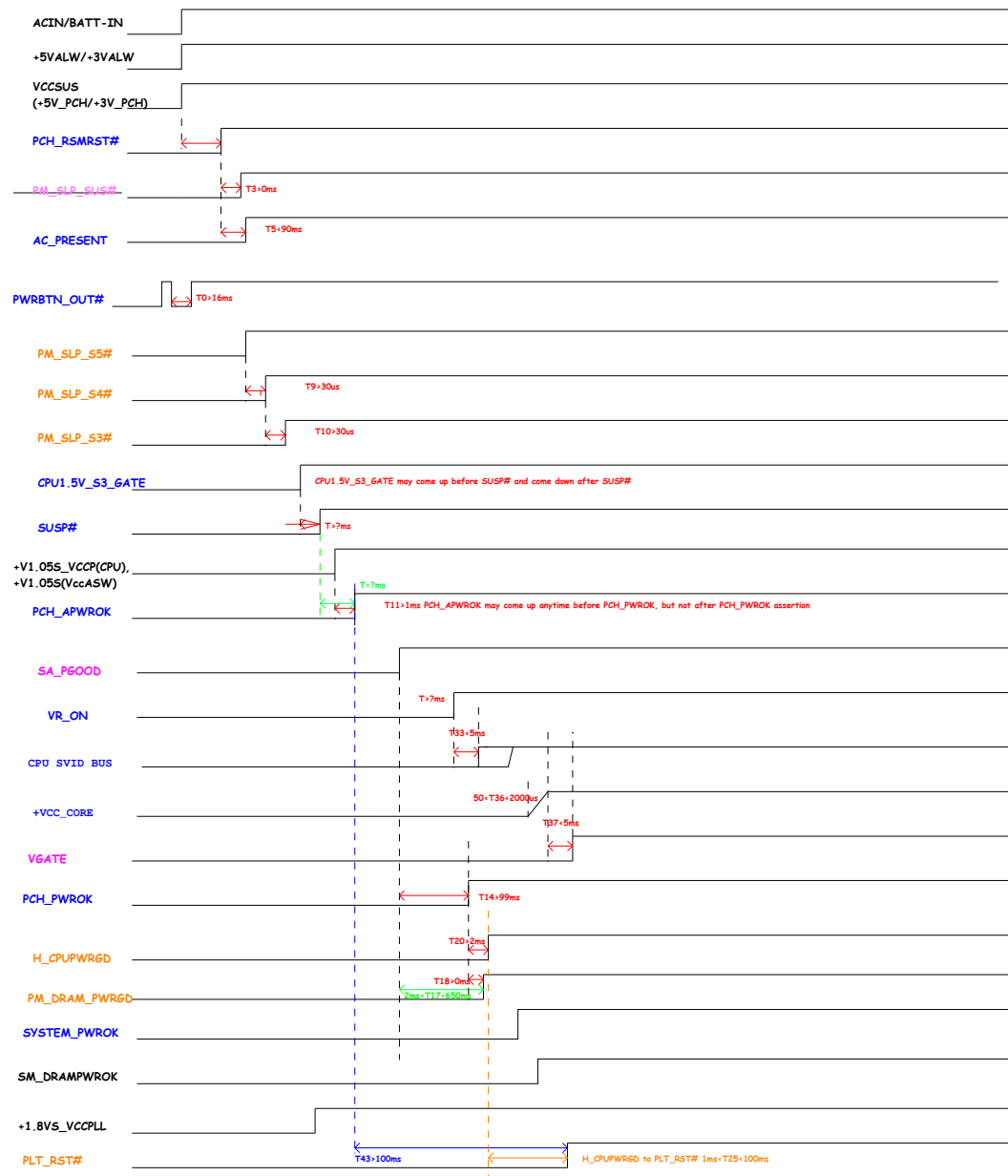


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Issued Date	2010/08/03	Deciphered Date	2012/12/31	Title	POWER BLOCK DIAGRAM
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1.	51.52	modify CPU soultion to 2+1	20120522	daniel_kao	only support BGA1023 35W		
2	43	Delete 51_ON circuit	20120522	daniel_kao	EC : 9012		
3	46	change 1.8v to SY8032A	20120522	daniel_kao			
4	45	change 3v/5v to RT8243A.	20120522	daniel_kao			
5	43	delete G718 circuit.	20120522	daniel_kao	follow EC 9012		
6	44	change EMI ISN Choke (PL102) to SH00000MW00.	20120522	daniel_kao			
7	53	Follow BGA1023 request, modify output MLCC count.	20120522	daniel_kao			
8	44	change pr101 from 2512 to 1206	20120523	daniel_kao			
9	45	Change pq304 from AON7406L to AON4468L change pq332 form AON7518 to AON7408L change pq306 from AON7212L to FDMC7692S change pl305 to 2.2UH +-20% ETQP3W2R2WFN 8.5A	20120523	daniel_kao			

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# Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER01		CPU change from socket to BGA 1023	0.1	4~9	CPU change to UCPU1(BGA1023) from JCPU1(socket).	5/28	
		Modify CPU Cap.	0.1	8,9	Change C74,C75 to 1uf/0402 Del C79,C80,C81,C82,C83,C84. Add C243,C239,C151,C177,C219,C157,C181,C237, C153,C192 to 1uF/0402 Add C238,C241,C240,C236,C156,C244,C242,C143 to 10uF/0603 Del C86,C87,C88,C89,C94. Add C245,C246,C254,C248,C249, to 1uF/0402. Add C253,C250,C252,C251,C247 to 10uF/0603.	5/28	
ER02		For Green CLK	0.1	12 13 32 20 43	Add R683 0 ohm. (PCH_32K) Add R637 0 ohm. (PCH_25M) Add R555 0 ohm. (LAN_25M) Add R96 0 ohm. (VGA_27M) Add C89 2.2uF. Add C86,C87 12pF. Add C81 22uF. Add C79,C83,C84,C82,C80 0.1uF. Add Y5 25M. Add U6 SLG3NB300VTR. Add R31 1M. Add R5 22ohm. Add R95,R35 33ohm. Add R30 330ohm. Add R97 0ohm.	5/28	
ER03		Remove reserve components	0.1	33 39 35 38 5,6,13, 17,18	Del C504,C505,C507. Del C655,C656,R681. Del C626,C628,C634,F1,Q53,Q56,R643,R664. Del D30,Q30,R532,R530. Del R267,R43,R750,R278,R290.	5/29	
ER04		Remove ASM1042 ( Del page 36) Green CLK VDD change EMI solution	0.1	13,36,37 43 13,32,20	Del ASM1042 . U6 VDD change to +3V_PCH from +LAN_IO. Add R185,R186,R187. (reserve) Add C255,C256,C257. (reserve)	5/30	
ER05		EMI solution	0.1	42	Add C258,C259,C260. (reserve)	5/31	
ER06		BOM modify	0.1	17 15	C180 change to 22uf (SE000000I110). stuff R234 0 ohm	6/4	
ER07		Green CLK modify  EMI solution	0.1	42  38	Del R31,R97. Change U6 pin3 voltage to +1.05VS. Add C261. (reserve)	6/4	
ER08		Modify Cap.	0.1	09	Add C262,C263 to 10uf . un-stuff C97,C85,C78 .	6/6	
PR01		Change JDIMM1. footprint	1.0	10	Change JDIMM1 footprint. (TYCO_2-2013298-1_204P)	7/4	
PR02		Swap Resistor	1.0	07	Swap R48 & R46.	7/5	
PR03		EMI solution / GCLK	1.0	35,42	Add C655,C656,C674 to 2.2pf . C87 change to 15pf. R95 change to 0 ohm.		

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